IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of	
Amos Intrater et al.	
Patent No. 5,630,153	TRANSMITTAL LETTER
Issued: May 13, 1997	
For: **INTEGRATED DIGITAL SIGNAL PROCESSOR/GENERAL PURPOSE CPU WITH SHARED INTERNAL MEMORY**	2001 Ferry Building San Francisco, CA 94111 (415) 433-4150 Attorney Docket No.: NSC8-8400

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith is an application for reissue of U.S. Patent No. 5,630,153 issued on May 13, 1997 for INTEGRATED DIGITAL SIGNAL PROCESSOR/GENERAL PURPOSE CPU WITH SHARED INTERNAL MEMORY.

CERTIFICATION UNDER 37 CFR §1.10

I hereby certify that this Reissue Application and the documents referred to as enclosed herein are being deposited with the United States Postal Service on this date January 20, 1999 in an envelope bearing "Express Mail Post Office to Addressee," Mailing Label Number EL151571733US, addressed to: Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231-0001.

(Howard Wong)

Enclosed are the following:

(1) Specification and claims (20 pages), and abstract (1 page);

(2) Declarations from Amos Intrater, Moshe Doron, Gideon Intrater, Lev Epstein, Maurice Valentaten, and Israel Greiss;

(3) Request for transfer of drawings for reissue application and provision of eight (8) temporary drawings (no changes in the drawings upon which the original patent was issued are to be made);

(4) Power of attorney by assignee;

(5) Offer to surrender original U.S. patent, United States Patent 5,630,153, Assent of assignee to reissue, and §3.73(b) compliance; and

(6) Information Disclosure Statement with one reference.

(7) Fee Calculation:

CLAIMS AS FILED

Number Filed		Number Extra	Rate		Basic Fee (1.16(h)) $760
Total Claims	41	- 20 21	X 18 (1.16(j))	=	$378
Independent Claims	8	- 3 5	X 78 (1.16(i))	=	$390

Filing fee Calculation $ 1,528

(8) A check is enclosed for $1,528.

(9) The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Deposit Account 12-1420. A duplicate of this transmittal is enclosed for this purpose.

Respectfully submitted,

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INTEGRATED DIGITAL SIGNAL PROCESSOR/GENERAL PURPOSE CPU WITH SHARED INTERNAL MEMORY

This is a continuation of application Ser. No. 08/011,102 filed on Jan. 29, 1993, now abandoned, which is a continuation of application Ser. No. 07/467,148 filed on Jan. 18, 1990 now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to data processing systems and, in particular, to a processing platform that provides integrated general purpose and digital signal processing (DSP) capabilities for recovering and processing digital data utilizing an internal shared memory resource.

2. Discussion of the Prior Art

The basic function of any communications system is to transmit information over a communication channel from an information source to a destination as fast and as accurately as possible.

There are two general types of information sources. Analog sources, such as a telephone microphone, generate a continuous signal. Digital sources, such as a digital data processing system, generate a signal that consists of a sequence of pulses.

Communications channels that are designed to transmit analog signals (e.g., the telephone network) have characteristics which make it difficult for them to transmit digital signals. To permit the transmission of digital pulse streams over an analog channel, it is necessary to utilize the digital data pulses to modulate a carrier waveform that is compatible with the analog transmission channel.

The equipment that performs the required modulation is generally referred to as a "MODEM". The term "MODEM" is an acronym for MOdulator-DEModulator, since one piece of equipment typically includes the capability not only to modulate transmitted signals, but also to demodulate received signals to recover the digital data from the modulated analog carrier waveform.

While passing through the transmission channel, the modulated carrier waveform suffers from distortion introduced both by the system itself and by noise contamination. Thus, one of the tasks of the modem's demodulation function is to filter the signal received from the transmission channel to improve the signal-to-noise ratio. The demodulator also retrieves timing information from the received signal to provide sampling points for recovering the digital data. The demodulator may also condition the data in other ways to make it suitable for additional processing.

In a conventional modem, the signal filtering, sampling and conditioning tasks are performed by three functional units: analog-to-digital conversion circuitry ("analog front end") that converts the received modulated carrier waveform to a digitized replica, a digital signal processor (DSP) that recovers the digital data from the digitized replica, and a control function for controlling both the analog front end and the digital signal processor. The digital signal processor recovers the data by implementing a signal conditioning and data recovery algorithm that is specific to the type of data being received.

For example, the digital signal processor function in a facsimile (fax) machine modem implements a special purpose algorithm that can only be used for recovering digital fax data. In the case of a fax system, the data to be recovered

is a digital bit map that corresponds to the transmitted hard copy image and which has been compressed to facilitate efficient transmission. The algorithm implemented by the digital signal processor function of the receiving fax machine's modem is a dedicated "fax" algorithm that has been designed specifically for accurately recovering the compressed bit map. It cannot recover digital data in a format other than a compressed bit map, e.g. voice mail data or data modem applications. A different digital signal processor implementing a different dedicated "voice mail" or "data modem" algorithm is needed for each of these other applications.

As shown in FIG. 1, a conventional fax machine architecture may be partitioned into two major functional blocks: (1) a special purpose fax modem block of the type described above for recovering a compressed bit map from a modulated carrier waveform and (2) a general purpose processor block for performing those tasks require to convert the compressed bit map to a corresponding hard copy image.

A well known example of a special purpose fax modem block is the Rockwell R96DFX MONOFAX® modem chip, the so-called "Rockwell Module". In the Rockwell Module, the incoming modulated carrier waveform received from an analog channel, i.e., a telephone line, is processed by an analog front end which generates a digitized replica of the analog signal; that is, the analog front end generates a digital reading of the input voltage level. A dedicated fax digital signal processor then performs the adaptive filtering, signal sampling, synchronization and carrier phase/frequency tracking required to reconstruct the compressed facsimile bit map from the digitized replica provided by the analog front end. The recovered bit map is then provided to the general purpose processor block which performs the additional processing functions required for printing the transmitted image. That is, the general purpose processor block controls and performs the data decompression, decoding, imaging and printing functions necessary to generate a hard copy reconstruction of the recovered bit map.

To transmit an image, the fax machine shown in FIG. 1 performs the above-described steps in reverse order. The general purpose processor block controls and performs the conversion of the hard copy image to a corresponding compressed bit map. The compressed bit map is then provided to the special purpose fax modem block which utilizes the bit map to modulate a carrier waveform which is transmitted over the analog channel to a destination fax machine.

A modem architecture similar to that of the Rockwell Module is also provided by the Yamaha YM7109 FAX modem LSI chip.

The fax machine architecture exemplified by the Rockwell Module and the Yamaha modem chip, that is, a special purpose fax modem block in combination with a separate general purpose processor block, suffers from a number of disadvantages. First, the system requires two separate processor functions: the special purpose DSP function of the modem block for recovering the compressed bit map and the general purpose processing and control functions of the general purpose processor block for performing the remaining tasks required to convert the compressed bit map to hard copy. Since there are periods of time when no facsimile transmissions are being received, the system's full processing capability is greatly underutilized. Furthermore, the DSP functions of the modem block are dedicated to a particular application, in this case, facsimile reception/transmission. That is, as stated above, the DSP algorithm utilized to

recover the incoming data is fixed; aside from the ability to modify the coefficients of the "fax" algorithm, there is no flexibility in the modem algorithm to allow it to perform tasks other than facsimile data recovery. This results in a high-cost, application-specific system architecture with redundant processing capabilities.

A variation in the Rockwell and Yamaha modem architectures is exemplified by the OKI KV96-X6D modem chip set. While the architecture of the OKI modem chip set maintains the separate modem and general purpose processor functions of the Rockwell and Yamaha modems described above, its analog front end and DSP functions are also separated. Since the DSP function is programmable, some flexibility in the type of signal that may be processed is permitted. However, once programmed, the DSP function of the OKI modem still relies on a fixed DSP algorithm. Thus, the OKI architecture has the same basic limitations and inefficiencies as the Rockwell and Yamaha devices.

The Texas Instruments TMS320C25 Digital Signal Processor provides a "general purpose" DSP capability in that it can accommodate a number of DSP algorithmic sequences. However, it relies on dedicated memory for storage of its DSP operations and data. Thus, it must incorporate its own segregated control capability aside from that provided by the general purpose processor with which it is associated.

NEC IC Microsystems Ltd. provides a modem DSP chip that includes a DSP core that is integrated with a general purpose processor block. However, the DSP core of the NEC device is dedicated to a particular algorithm and relies on its own control functions and an internal memory separate from that of the general purpose processor function for storage and retrieval of its operands. Furthermore, the general purpose processor function is fully embedded, making it unavailable for tasks other than those related to the dedicated DSP function.

It would, therefore, be desirable to have available a dual processor platform that can execute a variety of DSP algorithms while maintaining full general purpose processor capability.

SUMMARY OF THE INVENTION

The present invention provides a data processing system that utilizes integrate general purpose processor (GPP) and digital signal processor (DSP) functions that are connected for common access to an internal shared memory array. The shared memory array stores the operands for a set of basic DSP operations that can be executed by the DSP function. The sequence of DSP operations to be executed by the DSP function is selectively configurable by the GPP function; that is, the general purpose processor can define a variety of DSP algorithms that can be executed by the DSP function for processing different digital input signal formats. In addition to storing the operands required by the DSP function for execution of a DSP algorithm, the internal shared memory array also stores selected instructions and data required by the GPP function for execution of general purpose tasks. The operands, instructions and data may be selectively loaded to the internal shared memory array from system memory. After execution of a DSP algorithm, the corresponding information set may be down-loaded from the internal memory array to system memory and a new information set retrieved for execution of a subsequent DSP algorithm or a new general purpose processor task.

Thus, in accordance with the principles of the present invention, the general purpose processor selects a DSP

algorithm for conditioning and recovering digital data from the incoming signal. That is, the GPP selects from the set of basic DSP operations to define a specific sequence of DSP operations appropriate for processing the incoming signal. The GPP then retrieves operands required for execution of the selected DSP algorithm and/or instructions and data critical to the GPP for controlling the DSP function or for performing GPP tasks and loads them into the internal shared memory array. Next, the GPP invokes the first DSP operation in the selected sequence and the DSP function performs the DSP operation utilizing operands retrieved by the DSP function from both the shared memory array and system memory. Upon completion of the DSP operation by the DSP function, the GPP function either reads the result of the DSP operation, invokes the next DSP operation in the selected sequence or performs a GPP task. This process continues until the selected sequence of DSP operations has been executed by the DSP function. The GPP may then download from the internal shared memory array the operands, instructions and data utilized in executing the selected DSP algorithm and either identify and execute a subsequent DSP algorithm fashioned from the set of basic DSP operations or retrieve instructions and data required for a separate GPP task.

While the input signal to the data processing system may be received directly from a digital source, a preferred embodiment of the invention includes an analog front end that converts a modulated input signal received on an analog channel to a corresponding digital signal for processing by the data processing system.

Thus, a data processing system in accordance with the present invention provides a unique system partitioning by integrating a small DSP module and a general purpose processor. This unique partitioning provides a single processor solution for both DSP and general purpose computations that can utilize the same programming mode and the same system development tools for both functions. The DSP module provides the capability necessary to handle a variety of DSP requirements. The internal shared memory allows the DSP algorithms to be tuned or changed or new algorithms to be added to meet changing, expanding system requirements; general purpose computation intensive tasks can also be executed directly from the internal shared memory.

A better understanding of the features and advantages of the present invention may be obtained by reference to the following detailed description of the invention and accompanying drawings which set forth an illustrative embodiment in which the principles of the invention are utilized.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating the basic functional partitioning of a conventional facsimile system.

FIG. 2 is a block diagram illustrating the basic functional partitioning of a data processing system in accordance with the present invention.

FIG. 3 is a block diagram illustrating the primary functional units of a data processing system in accordance with the present invention,

FIG. 4 is a block diagram illustrating a DSP module utilizable in a data processing system in accordance with the present invention.

FIG. 5 illustrates the general purpose processor address mapping of a data processing system in accordance with the present invention.

FIG. 6 is a table illustrating the memory organization of a complex vector for use in a DSP module in accordance with the present invention,

FIG. **7** provides an instruction set summary for a DSP module in accordance with the present invention,

FIG. **8** is a table illustrating the handling of cyclic buffers for a DSP module in accordance with the present invention,

FIG. **9**A is a block diagram illustrating an internal bus configuration of a data processing system in accordance with the present invention with the DSP module executing a VCMAG command.

FIG. **9**B is a block diagram illustrating an internal bus configuration of a data processing system in accordance with the present invention with the DSP module executing a VCMAD, VCMUL or VCMAC command,

FIG. **9**C a block diagram illustrating an internal bus configuration of a data processing system in accordance with the present invention with the general purpose processor executing a read or write to registers of the DSP module or to the internal memory array.

DETAILED DESCRIPTION OF THE INVENTION

FIG. **2** shows a data processing system **10** which is uniquely partitioned in accordance with the concepts of the present invention. The data processing system **10** is described below in the context of the requirements of a facsimile system. However, it will be understood by those skilled in the art that the principles of the invention are applicable to any system which receives an incoming data signal that requires digital signal processing.

The data processing system **10** shown in FIG. **2** includes two primary functional elements: an analog front end **12** and an integrated processing platform **14**. The integrated processing platform **14** includes both a digital signal processor (DSP) module **16** and a general purpose processor (GPP) **18**.

The analog front end **12** converts a modulated input signal received from an analog transmission channel, e.g. a telephone line, to a digitized replica of the modulated input signal. The analog front end **12** can be implemented utilizing conventional, off-the-shelf integrated circuit products available for this purpose.

As stated above, the integrated processor platform **14** includes a DSP module **16** that recovers digital data from the digital signal generated by the analog front end **12**. The DSP module **16** includes a processing mechanism, described in greater detail below, that conditions the digital signal utilizing an algorithm comprising a selected sequence of DSP operations.

The general purpose processor **18** controls the DSP module **16** and processes the digital data generated by the DSP module **16** to a desired end result. The general purpose processor **18** may be any conventional state-of-the-art microprocessor.

As further shown in FIG. **2**, while in many applications, the analog front end **12** will be utilized to convert a modulated input signal received on an analog channel to a corresponding digital signal, there are a growing number of applications (e.g., ISDN and T1) in which a digital input signal will be received by the integrated processor platform **14** directly from a digital source.

Referring to FIG. **3**, both the DSP module **16** and the general purpose processor **18** are connected to an internal bus **20**, allowing both the DSP module **16** and the general purpose processor **18** to communicate with a system memory (not shown) via a conventional bus interface unit **24** for transfer of control/status information and addresses/data therebetween. It will be understood by those skilled in the art

that the internal bus **20** comprises both an internal address bus for handling address references by the DSP module **16** and the general purpose processor **18** and an internal data bus for handling instruction and data transfers.

To save bus bandwidth, the DSP module **16** stores operands used in executing DSP algorithms in an internal RAM memory array **22** which, as will be described in greater detail below, is also accessible to general purpose processor **18**. That is, in accordance with the concepts of the present invention, the internal memory array **22** serves as a shared resource for both the DSP module **16** and the general purpose processor **18**. In the illustrated embodiment, the internal memory is shown as accessible by the DSP module **16** and the general purpose processor **18** via the internal bus **20**. It will be understood by those skilled in the art that other bus structures would also provide the desired shared accessibility to the internal memory array **22**; for example, the internal memory array **22** could be implemented as a dual port memory.

As described in greater detail below, the DSP module **16** may fetch operands in parallel from the internal memory array **22** and system memory.

The DSP module **16** executes vector operations on complex variables that are optimized for DSP applications. The general purpose processor **18** treats the DSP module **16** as a memory mapped I/O device that occupies a reserved memory space, interfacing with the DSP module **16** via a set of memory mapped registers.

As shown in FIG. **4**, high performance is achieved in the DSP module **16** by using the internal shared memory array **22** as well as a multiplier/accumulator **26**. The DSP module also includes its own internal address generator **28** for system memory and internal operand accesses, thus reducing the load on the general purpose processor **18**. Both the multiplier/accumulator **26** and the address generator **28** are conventional implementations.

In the operation of the data processing system **10**, the general purpose processor **18** selects from a basic set of DSP operations to define a specific sequence of operations as the DSP algorithm to be executed by the DSP module **16** for recovering data from the incoming digital signal. The general purpose processor then retrieves operands required for execution of the selected DSP algorithm and/or instructions and data critical to the general purpose processor for controlling the DSP module **16** or for performing general purpose tasks and loads them into the internal RAM array **22**. The general purpose processor then invokes the first DSP operation in the selected sequence by issuing the corresponding command to the control register of the DSP module **16**. The DSP module then places the general purpose processor **18** in a continuous wait state while it performs the first DSP operation utilizing operands retrieved by the address generator **28** from the RAM array **22** and system memory. Upon completion of the DSP operation, the DSP module cancels the continuous wait state and the general purpose processor **18** then either reads the status of the DSP module **16** or the result of the DSP operation or carries on with the execution of its normal program flow, which may be either invoking the next DSP operation in the selected sequence by issuing the appropriate command to the DSP module control register or performance of a general purpose task. This process continues until the selected sequence of DSP operations has been completed. The general purpose processor may then download the contents of the shared internal RAM array **22** and retrieve a new set of operands, instructions and data for further DSP operations or general purpose processing tasks.

As further shown in FIG. 4, the DSP module 16 performs complex arithmetic calculations on two vector operands provided to the multiplier/accumulator 26 at Port Y and Port D. One vector is retrieved from the internal memory array 22. The other vector is either organized as a circular buffer in the system memory (described in greater detail below) or retrieved from the internal memory array 22.

The DSP module 16 executes vector operations in a two stage pipeline. This allows for a significant performance enhancement as the fetch and execution of operands for consecutive vector elements are performed simultaneously rather than in a strictly sequential manner. The DSP module 16 can fetch up to two data elements at a time, using its address generator 28 for system memory access and the internal array 22 for the second operand. While fetching operands for one vector element, the DSP module 16 performs the multiply and add operations on the previous vector element.

The DSP module 16 contains seven registers in addition to the RAM array 22. These registers, as well as the internal memory array 22, are accessed by the general purpose processor 18 as memory-mapped I/O devices. As shown in FIG. 5, their associated addresses reside in the upper part of a 32-bit address range of general purpose processor 18. External memory locations are specified by the lower 24 address bits and mapped to the lower 16 megabyte of this address range.

Any reference by general purpose processor 18 to the registers of the DSP module 16 or to the internal memory array 22 is done using a bus protocol for internal control register access to enable external observability. This protocol is more fully described in commonly-assigned U.S. patent application Ser. No. 07/750,771, filed Aug. 8, 1991, now U.S. Pat. No. 5,212,775, which is a continuation of U.S. patent appliction Ser. No. 07/461,023, filed Jan. 4, 1990, by Zeev Bikowsky and Dan Biran, titled METHOD AND APPARATUS FOR OBSERVING MEMORY-MAPPED REGISTERS, now abandoned; the just-referenced Bikowsky/Biran application is hereby incorporated by reference to provide additional background information regarding the present invention.

Each storage location in the internal memory array 22 is 32 bits wide and holds one complex number.

As stated above, the internal memory array 22 is not limited to storage of filtering coefficients for a specific DSP algorithm. It can also be used as a fast, zero-wait state, integrated memory for storing instructions and data utilized by the general purpose processor 18 as well as for storing selected operands for use by the DSP module 16 for processing a variety of data signal formats.

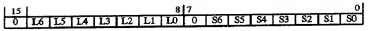
The memory array 22 can be used for instruction fetches with only one restriction: instructions must be loaded into the array 22 using word aligned accesses. This can be achieved by moving the aligned double-word from system memory to memory array 22. Data can also be stored in the memory array 22 with one restriction: storing data in the array 22 can be done only if all the data is written using aligned word or double-word accesses.

Referring back to FIG. 4, the multiplier input register Y is a 32-bit register that holds one complex operand. The multiplier input register Y is mapped into two consecutive words called **Y0** and **Y1**.

The accumulator register A is a 32-bit register that holds one complex result. The A register is mapped into consecutive words, also called **A0** and **A1**. Internally, **A0** and **A1** are 32-bit registers. However, only bits **15–30** (i.e., 16 bits) are visible. The rest of the bits are used for a higher dynamic range and intermediate calculations.

A 24-bit pointer to the beginning of the data vector in the external system memory is provided by data pointer register DPTR. In order to implement circular buffers, only the less significant bits of the DPTR pointer are incremented. When the end of a buffer is reached, the least significant bits of the DPTR pointer are reloaded with zeroes. The number of bits that are set to zero, which defines the size of the circular buffer, is controlled by a Control Register CTL, which is described below. The least significant word of the DPTR pointer is called **DPTR0** and the most significant byte is called **DPTR1**.

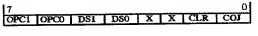
The CPTR register holds the address and length of the coefficient vector.



S0–S6 Start Address of coefficient's vector (number of C reg.)

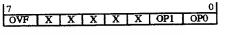
L0–L6 Length of coefficient' vector (in double words).

The Control Register CTL controls the various modes of operation of the data processing system **10**.



OPC1–0 Operation code.
00 VCMAD Vector Complex Multiply Add
01 VCMUL Vector Complex Multiply
10 VCMAC Vector Complex Multiply Accumulate
11 VCMAG Vector Complex Magnitude
DS0–DS1 Data Buffer Size.
00 8 double-words
01 16 double-words
10 32 double-words
11 64 double-words
CLR Clear Accumulator (A0 and A1) before beginning the operation.
COJ Conjugate when set to 1, the value of the operand in Port D of the multiplier will be conjugated prior to multiplication.

The Status Register ST holds the status of the last vector operation.



OP0 Overflow occurred on calculation of A0.
OP1 Overflow occurred on calculation of A1.

The ST register is cleared to 0 in the following cases:
the user writes directly to either **A0** or **A1**.
the user writes to the CTL register upon reset.

The operation of the DSP module **16** will now be described in greater detail; the following terms will be used in the operational description:

C[i]	an entry in internal memory array 22, entry [i] can be selected by address generator 28 or directly accessed by CPU 18;
D[i]	Data from system memory fetched using address generator 28;
Y	Complex Multiplier input register 30 in FIG. 4;
D[i]*	The conjugate of D[i];
A	Complex Accumulator register.

The DSP module **16** executes the following six basic commands:

VCMAC	Vector Complex Multiply Accumulate
VCMAG	Vector Complex Magnitude
VCMAD	Vector Complex Multiply Add
VCMUL	Vector Complex Multiply
LOAD	Write into C, Y, A or CTL
STORE	Read from C, Y, A, ST or CTL

The VCMAC, VCMAD and VCMUL commands use the following parameters:

D	Vector Start Address in system memory
C	Vector Start Address in internal RAM
	Vector Length
	Control bits

The VCMAG command uses only the last three operands.

Complex numbers are organized in the internal memory array **22** as double words. Each double word contains two 16-bit 2's complement fractional integers. The less significant word contains the Real part of the number. The most significant word contains the Imaginary part of the number.

The complex vectors utilized by the DSP module **16** consist of arrays of complex numbers stored in consecutive addresses. Complex vectors must be aligned to double word boundary. FIG. **6** illustrates the memory organization of a vector D.

Referring back to FIG. **4**, the arithmetic logic unit 26 of the DSP module **16** contains a 16×16 multiplier **26***a* and a 32-bit adder/accumulator **26***b*. Bits **15–30** (16 bits) of the result are rounded and can be read by accessing the A register. If an overflow is detected during an operation, the Status Register (ST) overflow bit and either the OP**0** bit or the OP1 bit is set to "1."

When data is loaded into the adder/accumulator **26***b*, the 16 bits of data are loaded into bits **15–30**, the lower bits are set to "0", while bit **31** gets the same value as bit **30** (sign extended). An overflow is detected whenever the value of bit **30** is different from the value of bit **31**.

Each basic DSP operation or instruction to be performed by the DSP module **16** is controlled by two OP-code bits (OPC**0** and OPC1) and two specifiers (COJ and CLR). COJ specifies whether the operand on port D of the multiplier **26***a* must be conjugated prior to multiplication. The CLR bit is used to extend the instruction set. On VCMAC and VCMAG, CLR specifies whether the accumulator **26***b* must be cleared at the beginning of the vector operation. On VCMAD, CLR specifies that the operation will ignore the value of C[i]. In VCMUL, CLR indicates that the value of D[i] is to be taken instead of 1+D[i].

FIG. **7** provides a summary of the set of basic DSP operations executed by the DSP module **16** as a function of

the OPC1, OPC0, COJ, and CLR bits in the CTL register. In FIG. 7, "SIGMA" represents the summation sign:

$$\sum_{i=1}^{M}$$

All the operands are complex numbers. Thus, A=SIGMA C[i]×D[i] breaks down to:

$$Re(A)=\text{Sigma}\{Re(C[i])\times Re(D[i])+Im(C[i])\times Im(D[i])\}$$

$$Im(A)=\text{Sigma}\{Re(C[i])\times Im(D[i])+Im(C[i])\times Re(D[i])\}$$

The accumulator **26***b*, the multiplier input register Y, the external data pointer DPTR and the coefficient pointer CPTR registers are used as temporary registers during vector operations. Values stored in these register prior to activation of the DSP module **16** are destroyed. If the content of the accumulator register A after an operation of the DSP module **16** is used as an initial value for the next operation, it must be remembered that the least significant bits of (**0/14**) may contain a value of other than zero.

As stated above, the DSP module **16** accesses arrays of data in external memory using the DPTR pointer as an address. The DS**0** and DS1 bits of the CTL register control the size of the array. The DSP module **16** allows a convenient way of handling data arrays as a FIFO. Only the appropriate number of the least significant bits of the DPTR are incremented on each access. The upper bits remain constant. FIG. **8** shows which bits are incremented. The rest remain constant.

FIG. **9**A illustrates the operation of the data processing system **10** with the DSP module **16** executing the VCMAG command while the general purpose processor **18** executes a general purpose task.

As shown in FIG. **9**A, bidirectional switches S that are responsive to control signals provided by the general purpose processor **18** are located on the internal bus **20** so as to permit configuration of a variety of communications paths among the DSP module **16**, the general purpose processor **18** and the bus interface unit **24** (which, as stated above, provides access to external memory).

When the DSP module **16** is executing the VCMAG command, the DSP module **16** is .isolated from the internal bus **20** so that the address generator **28** can retrieve operands for the VCMAG operation from the internal memory array **22** for both port Y and port D of the multiplier/accumulator **26**. Isolation of the DSP module **16** in this manner allows the general purpose processor **18** to reference the external memory via the bus interface unit **24** to allow transfer of data and instructions between the general purpose processor **18** and external memory for simultaneous execution of a general purpose task.

FIG. **9**B illustrates the bus configuration during execution of the VCMAD, VCMUL or VCMAC commands by the DSP module **16**. In this case, the address generator **28** references an operand stored in the memory array **22** which is then provided to the Y port of the multiplier/accumulator **26**. The address generator **28** also references a location in external memory which provides the second operand to the D port of the multiplier/accumulator **26**. The general purpose processor **18** is isolated from both the internal memory array **22** and external memory.

FIG. **9**C illustrates read and write operations by the general purpose processor **18** either to the Y register or the accumulator register A or to the internal memory array **22** of the DSP module. As shown in FIG. **9**C, in this case, the

general purpose processor 18 references the selected storage element as memory mapped I/O via the internal address bus and either reads or writes to the selected storage element via the internal data bus.

Addition information regarding the present invention is provided in National Semiconductor Corporation's Advanced Data Sheet, NS32FX16, High Performance Fax Processor, which is provided as Appendix A at the end of this Detailed Description of the Invention.

It should be understood that various alternatives to the embodiments of the invention described herein may be employed in practicing the invention. It is intended that the following claims define the scope of the invention, that the structure and methods within the scope of these claims and their equivalence be covered thereby.

What is claimed is:

1. A data processing system for processing a digital signal, the data processing system comprising:

a shared bus for transferring both data and instructions;

a shared memory array for storing both data and general purpose instructions and that is connected for transfer of both data and general purpose instructions between the shared bus and the shared memory array;

a digital signal execution unit connected to the shared bus for processing the digital signal utilizing both data transferred between the shared memory array and the digital signal execution unit on the shared bus and a selected sequence of individual digital signal processor (DSP) instructions, the selected sequence of DSP instructions consisting of individual general purpose instructions transferred between the shared memory array and the digital signal execution unit on the shared bus; and

a general purpose processor connected to the shared bus for controlling the digital signal execution unit by selecting each general purpose instruction to be transferred to the digital signal execution unit from the shared memory array

whereby the selected sequence of individual DSP instructions executed by the digital signal execution unit is selectively configurable by the general purpose processor.

2. An integrated circuit data processing system for processing a digital signal, the data processing system comprising;

a shared internal bus for transferring both general purpose instructions and data;

a shared bus interface unit connected to the shared internal bus and connectable via a shared external bus to a shared external memory array via an external input/output port of the shared external memory array such that general purpose instructions and data stored in the shared external memory array may be transferred via external input/output port to be shared internal bus via the shared bus interface unit;

a digital signal execution unit connected to the shared internal bus for processing the digital signal utilizing both data transferred to the digital signal execution unit from the shared external memory array via the shared internal bus and a selected sequence of individual digital signal processor (DSP) instructions, the selected sequence of DSP instructions consisting of individual general purpose instructions transferred to the digital signal execution unit from the shared external memory array via the shared internal bus; and

a general purpose processor connected to the shared internal bus for controlling the digital signal execution

unit by selecting each of the general purpose instructions to be transferred to the digital signal execution unit from shared external memory array via the shared internal bus

whereby the selected sequence of individual DSP instructions executed by the digital signal execution unit is selectively configurable by the general purpose processor.

3. An integrated circuit data processing system as in claim 2 and further comprising a shared internal memory array connected to the shared internal bus via an internal input/output port of the shared internal memory array such that general purpose instructions and data stored in the shared internal memory are transferrable via the internal input/output port of the shared internal memory array to the shared internal bus for transfer to either the digital signal execution unit or the general purpose processor

whereby the selected sequence of individual DSP instructions executed by the digital signal execution unit is selectively configurable by the general purpose processor selecting individual general purpose instructions from the shared external memory and/or the shared internal memory.

4. A data processing system for processing a digital signal, the data processing system comprising:

a shared bus for transferring both data operands and general purpose instructions;

a shared memory array for storing both data operands and general purpose instructions and that is connected for transfer of data operands and general purpose instructions between the shared bus and the shared memory array;

a digital signal execution unit connected to the shared bus for processing the digital signal utilizing data operands transferred from the shared memory array to the digital signal execution unit on the shared bus and a selected sequence of individual digital signal processor (DSP) instructions, the selected sequence of DSP instructions consisting of individual general purpose instructions transferred from the shared memory array to the digital signal execution unit on the shared bus; and

a general purpose processor connected to the shared bus for controlling the digital signal execution unit by selecting each general purpose instruction to be transferred to the digital signal execution unit from the shared memory array; and

wherein the digital signal execution unit includes

a control register connected to the shared bus for storing a general purpose instruction transferred to the digital signal execution unit by the general purpose processor from the shared memory array on the shared bus;

a multiply/accumulate unit that responds to storage of said general purpose instruction in the control register by initiating execution of a DSP operation corresponding to said general purpose instruction; and

a DSP address generator connected to the shared bus for retrieving a first data operand stored in the shared memory and utilizable by the multiply/accumulate unit in executing said DSP operation.

5. A data processing system as in claim 4 wherein the multiply/accumulate unit includes first and second input ports for receiving said first data operand and a second data operand respectively, for utilization by the multiply/accumulate unit in executing said DSP operation.

6. A data processing system as in claim 5 wherein the address generator includes means for retrieving both said

first data operand and said second data operand from the shared memory array via the shared bus.

7. An integrated circuit data processing system for processing a digital signal, the data processing system comprising:

(a) a digital signal execution unit that recovers digital data from the digital signal by executing a selected sequence of digital signal processor (DSP) instructions;

(b) a general purpose processor that selects the sequence of DSP instructions for execution by the digital signal execution unit from a set of DSP instructions and that performs general purpose processing tasks by executing general purpose instructionsons utilizing selected data;

(c) a shared internal bus for transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected; and

(d) a shared internal memory array connected to the shared internal bus via an internal input/output port of the shared internal memory array such that the shared internal memory array is accessible by the digital signal execution unit via the internal input/output port for transferring operands utilizable by the digital signal execution unit between the shared internal memory array and the digital signal execution unit on the shared internal bus and such that the shared internal memory array is accessible by the general purpose processor via the internal input/output port for transferring the general purpose instructions and the selected data between the shared internal memory array and the general purpose processor on the shared internal bus; and

(e) a shared bus interface unit connected between the shared internal bus and a shared external system memory that stores operands, instructions and data for implementing the transfer of operands, instructions and data between the shared internal bus and the shared external system memory such that the digital signal execution unit and the general purpose processor may access either the shared internal memory via the internal input/output port of the shared internal memory or the shared external memory system via the shared bus interface unit.

8. A data processing system as in claim 7 wherein the digital signal execution unit includes an internal address generator for retrieving operands from either the shared internal memory array or the external memory system via the shared internal bus for use by the digital signal execution unit in executing the selected sequence of DSP instructions.

9. An integrated circuit data processing system for processing a digital signal, the data processing system comprising:

(a) a digital signal execution unit that recovers digital data from the digital signal by executing a selected sequence of digital signal processor (DSP) instructions;

(b) a general purpose processor that selects the sequence of DSP instructions for execution by the digital signal execution unit from a set of DSP instructions and that performs general purpose processing tasks by executing general purpose instructions utilizing selected data;

(c) a shared internal bus for transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected; and

(d) a shared internal memory array connected to the shared internal bus via an internal input/output port of the shared internal memory array such that the shared internal memory array is accessible by the digital signal execution unit via the internal input/output port for transferring operands utilizable by the digital signal execution unit between the shared internal memory array and the digital signal execution unit on the shared internal bus and such that the shared internal memory array is accessible by the general purpose processor via the internal input/output port for transferring the general purpose instructions and the selected data between the shared internal memory array and the general purpose processor on the shared internal bus;

wherein the digital signal execution unit includes an internal address generator for retrieving operands from the shared internal memory array via the shared internal bus for use by the digital signal execution unit in executing the selected sequence of DSP instructions.

10. An integrated circuit data processing system for processing a digital signal, the data processing system comprising:

(a) a digital signal execution unit that recovers digital data from the digital signal by executing a selected sequence of digital signal processor (DSP) instructions;

(b) a general purpose processor that selects the sequence of DSP instructions for execution by the digital signal execution unit from a set of DSP instructions and that performs general purpose processing tasks by executing general purpose instructions utilizing selected data;

(c) a shared internal bus for transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected;

(d) a shared internal memory array connected to the shared internal bus via an internal input/output port of the shared internal memory array such that the shared internal memory array is accessible by the digital signal execution unit via the internal input/output port for transferring operands utilizable by the digital signal execution unit between the shared internal memory array and the digital signal execution unit on the shared internal bus and such that the shared internal memory array is accessible by the general purpose processor via the internal input/output port for transferring the general purpose instructions and the selected data between the shared internal memory array and the general purpose processor on the shared internal bus;

wherein the DSP instructions and the general purpose instructions comprise subsets of a single instruction set executable by the data processing system; and

(e) an instruction sequencing unit connected to the shared internal bus for controlling the flow of execution of the DSP instructions and the general purpose instructions.

11. A data processing system comprising:

a first bus;

a memory connected to the first bus;

a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and

a digital signal processor (DSP) connected to the first bus, the DSP having a register and starting execution of an instruction in response to the GPP loading information into the register.

12. The data processing system of claim 11 wherein the operands held in the memory are randomly accessible.

13. The data processing system of claim 11 wherein the information placed in the register identifies the instruction to be executed.

14. The data processing system of claim 11 wherein the DSP is connected to the memory via a second bus.

15. The data processing system of claim 11 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

16. The data processing system of claim 11 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

17. The data processing system of claim 11 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

18. The data processing system of claim 11 wherein the DSP only executes a single instruction when said information is loaded into the register.

19. The data processing system of claim 11 wherein the DSP retrieves the operands from the memory.

20. A data processing system comprising:

a first bus;

a memory connected to the first bus;

a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and

a digital signal processor (DSP) connected to the first bus, the DSP having a register and executing an instruction in response to the GPP loading information into the register, the information loaded into the register identifying the instruction.

21. The data processing system of claim 20 wherein the operands held in the memory are randomly accessible.

22. The data processing system of claim 20 wherein the information placed in the register identifies the instruction to be executed.

23. The data processing system of claim 20 wherein the DSP is connected to the memory via a second bus.

24. The data processing system of claim 20 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

25. The data processing system of claim 20 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

26. The data processing system of claim 20 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

27. The data processing system of claim 20 wherein the DSP only executes a single instruction when said information is loaded into the register.

28. The data processing system of claim 20 wherein the DSP retrieves the operands from the memory.

29. A data processing system comprising:

a first bus;

a memory connected to the first bus;

a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and

a digital signal processor (DSP) connected to the first bus, the DSP having a register, executing an instruction in response to the GPP loading information into the register, and retrieving operands required by the instruction from the memory by processing the information loaded into the register.

30. The data processing system of claim 29 wherein the operands held in the memory are randomly accessible.

31. The data processing system of claim 29 wherein the information placed in the register identifies the instruction to be executed.

32. The data processing system of claim 29 wherein the DSP is connected to the memory via a second bus.

33. The data processing system of claim 29 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

34. The data processing system of claim 29 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

35. The data processing system of claim 29 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

36. The data processing system of claim 29 wherein the DSP only executes a single instruction when said information is loaded into the register.

37. A data processing system comprising:

a digital signal processor (DSP) that processes digital data by executing an algorithm that includes a specific sequence of DSP operations;

a general purpose processor (GPP) that selects the sequence of DSP operations for execution by the DSP from a basic set of DSP operations, and that performs general purpose tasks utilizing selected instructions and data;

a bus to which both the DSP and the GPP are connected;

a memory connected to the bus such that the memory is accessible by the DSP for retrieving operands utilized by the DSP in executing the selected sequence of DSP operations and by the GPP for loading operands required for execution of the selected DSP algorithm and/or instructions and data for use by the GPP for controlling the DSP; and

a control register of the DSP characterized in that said GPP invokes a first DSP operation in the selected sequence by issuing a corresponding command directly to said control register of the DSP.

38. The system of claim 37 wherein the DSP, in response to receiving a first DSP operation, places the GPP in a continuous wait state while the DSP performs the first DSP operation utilizing operands retrieved from the memory.

39. The system of claim 37 wherein, upon completion of execution of the selected sequence of the DSP operations, the GPP downloads contents of the memory and retrieves a new set of operands, instructions, and data for a new sequence of DSP operations.

40. A data processing system comprising:

a first data bus;

a second data bus;

a memory connected to the first data bus and the second data bus;

a general purpose processor (GPP) connected to the first data bus, the GPP loading operands into the memory via the first data bus; and

a digital signal processor (DSP) connected to the first data bus and the second data bus, the DSP executing an instruction identified by the GPP, and

retrieving operands from the memory via the second data bus.

41. The data processing system of claim 40 wherein the operands held in the memory are randomly accessible.

42. The data processing system of claim 40 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

43. The data processing system of claim 40 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

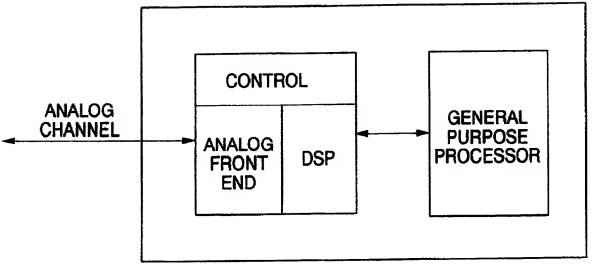
44. The data processing system of claim 40 and further comprising:

a bus interface unit connected to the first data bus; and

a third data bus connected to the bus interface unit.

[57] **ABSTRACT**

An integrated data processing platform for processing a digital signal that includes a general purpose processor and a digital signal processor (DSP) module. The DSP module recovers digital data from a digital signal utilizing a sequence of DSP operations selected by the general purpose processor. The general purpose processor processes the digital data recovered by the DSP module, but is also available to perform general purpose tasks. A shared internal memory array selectively provides information to the DSP module and to the general purpose processor. The information stored in the internal memory array includes operands utilized in the execution of the DSP algorithm and selected instructions and data utilized by the general purpose CPU either for controlling the execution of the DSP algorithm or for executing its own general purpose tasks. While in many applications the data processing system will include an analog front end that converts a modulated input signal received on an analog transmission channel to a corresponding digital signal for processing by the data processing system, the data processing system may also receive the digital signal directly from a digital source.



(PRIOR ART)
FIG. 1

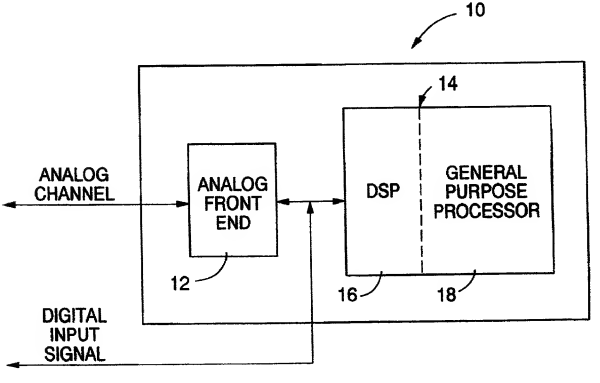


FIG. 2

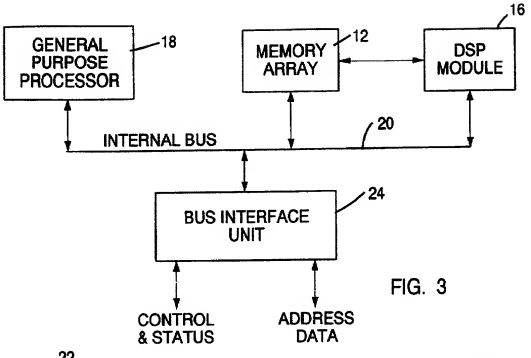

16
GENERAL PURPOSE PROCESSOR
18
MEMORY ARRAY
12
DSP MODULE
INTERNAL BUS
20
BUS INTERFACE UNIT
24
CONTROL & STATUS
ADDRESS DATA

FIG. 3

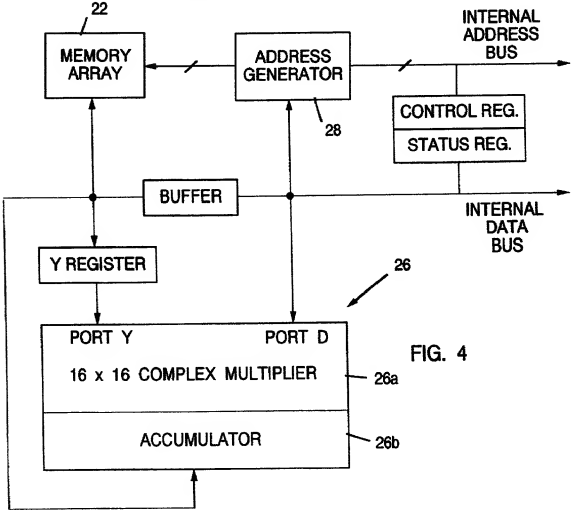

22
MEMORY ARRAY
ADDRESS GENERATOR
INTERNAL ADDRESS BUS
28
CONTROL REG.
STATUS REG.
BUFFER
INTERNAL DATA BUS
Y REGISTER
26
PORT Y
PORT D
16 x 16 COMPLEX MULTIPLIER
26a
ACCUMULATOR
26b

FIG. 4

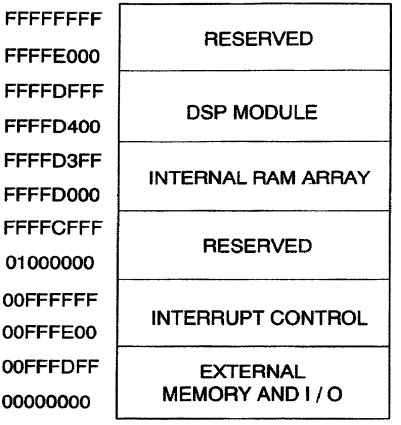

FFFFFFFF
FFFFE000
RESERVED
FFFFDFFF
FFFFD400
DSP MODULE
FFFFD3FF
FFFFD000
INTERNAL RAM ARRAY
FFFFCFFF
01000000
RESERVED
00FFFFFF
00FFFE00
INTERRUPT CONTROL
00FFFDFF
00000000
EXTERNAL MEMORY AND I / O

FIG. 5

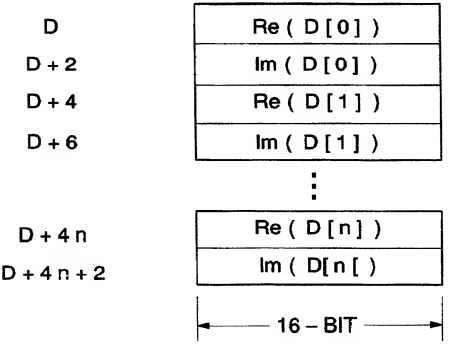

ADDRESS
CONTENTS
D
Re (D [0])
D + 2
Im (D [0])
D + 4
Re (D [1])
D + 6
Im (D [1])
D + 4 n
Re (D [n])
D + 4 n + 2
Im (D[n [ )
16 – BIT

FIG. 6

INSTRUCTION	OPC1	OPC0	CLR	COJ	OPERATION	CYCLES
VCMAD	0	0	0	0	C[i] <= C[i]+YxD[i]	9+(Nx8)
	0	0	0	1	C[i] <= C[i]+YxD[i]*	
	0	0	1	0	C[i] <= YxD[i]	
	0	0	1	1	C[i] <= YxD[i]*	
VCMUL	0	1	0	0	C[i] <= C[i]x(1+D[i])	9+ (Nx8)
	0	1	0	1	C[i] <= C[i]x(1+D[i]*)	
	0	1	1	0	C[i] <= C[i]xD[i]	
	0	1	1	1	C[i] <= C[i]xD[i]*	
VCMAC	1	0	0	0	A <= A + SIGMA(C[i]xD[i])	6+ (Nx8)
	1	0	0	0	A <= A + SIGMA(C[i]xD[i]*)	
	1	0	1	0	A <= SIGMA(C[i]xD[i])	
	1	0	1	1	A <= SIGMA(C[i]xD[i]*)	
VCMAG	1	1	0	0	A <= A + SIGMA(C[i]xC[i])	5+ (Nx8)
	1	1	0	1	A <= A + SIGMA(C[i]xC[i]*)	
	1	1	1	0	A <= SIGMA(C[i]xC[i])	
	1	1	1	1	A <= SIGMA(C[i]xC[i]*)	

FIG. 7

DS1	DS0	EXTERNAL BUFFER SIZE (DM)	CONSTANT ADDRESS BITS	INCREMENTED ADDRESS BITS
0	0	8	A0 , A5 – A23	A1 – A4
0	1	16	A0 , A6 – A23	A1 – A5
1	0	32	A0 , A7 – A23	A1 – A6
1	1	64	A0 , A8 – A23	A1 – A7

FIG. 8

GENERAL PURPOSE PROCESSOR
18
10
S
BIU
24
AD (0:15)
EXTERNAL SYSTEM MEMORY
INTERNAL ADDRESS BUS
CONTROL REG.
STATUS REG.
INTERNAL DATA BUS
26
ADDRESS GENERATOR
28
16
BUFFER
22
MEMORY ARRAY
Y REGISTER
PORT D
PORT Y
16 x 16 COMPLEX MULTIPLIER
ACCUMULATOR
26a
26b

FIG. 9A

MEMORY ARRAY
22
16
ADDRESS GENERATOR
28
BUFFER
Y REGISTER
PORT Y
16 x 16 COMPLEX MULTIPLIER
PORT D
ACCUMULATOR
26
26a
26b
INTERNAL ADDRESS BUS
CONTROL REG.
STATUS REG.
INTERNAL DATA BUS
10
S
GENERAL PURPOSE PROCESSOR
18
BIU
24
AD (0:15)
EXTERNAL SYSTEM MEMORY

FIG. 9B

GENERAL PURPOSE PROCESSOR
18
S
BIU
24
AD (0:15)
EXTERNAL SYSTEM MEMORY
10
INTERNAL ADDRESS BUS
INTERNAL DATA BUS
CONTROL REG.
STATUS REG.
26
26a
26b
PORT D
16 x 16 COMPLEX MULTIPLIER
ACCUMULATOR
PORT Y
ADDRESS GENERATOR
28
16
BUFFER
Y REGISTER
22
MEMORY ARRAY

FIG. 9C

Express Mail Label No.:
EL151571733US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of	)	
	)	
Amos Intrater et al.	)	
	)	**POWER OF ATTORNEY**
Patent No. 5,630,153	)	
	)	
Filed: May 13, 1997	)	
	)	
For: **INTEGRATED DIGITAL SIGNAL PROCESSOR/GENERAL PURPOSE CPU WITH SHARED INTERNAL MEMORY**	)	Attorney Docket No.: NSC8-8400

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

National Semiconductor Corporation hereby appoints the members of the firm of LIMBACH & LIMBACH L.L.P., a firm composed of:

Karl A. Limbach	18,689	Mark A. Dalla Valle	34,147	Kyla L. Harriel	41,816
George C. Limbach	19,305	Charles P. Sammut	28,901	Mayumi Maeda	40,075
John K. Uilkema	20,282	Mark C. Pickering	36,239	Kent J. Tobin	39,496
Neil A. Smith	25,441	Patricia Coleman James	37,155	Michael R. Ward	38,651
Veronica C. Devitt	29,375	Kathleen A. Frost	37,326	Steven M. Santisi	40,157
Ronald L. Yin	27,607	Alan S. Hodes	38,185	Charles L. Hamilton	42,624
Gerald T. Sekimura	30,103	Alan A. Limbach	39,749	Andrew V. Smith	43,132
Michael A. Stallman	29,444	Douglas C. Limbach	35,249	Heath W. Hoglund	41,076
Philip A. Girard	28,848	Brian J. Keating	39,520	William G. Goldman	42,590
Michael J. Pollock	29,098	Seong-Kun Oh*		J. Thomas McCarthy	22,420
Stephen M. Everett	30,050	Cameron A. King	41,897	Joel G. Ackerman	24,307
Alfred A. Equitz	30,922	* Recognition under 37 CFR 10.9(b)			

2001 Ferry Building, San Francisco, CA 94111, (415) 433-4150, FAX (415) 433-8716, and the following members of the National Semiconductor Corporation Intellectual Property Department:

Eugene Conser	39,149
Coleman Reif	38,593
Allen Tremain	40,207
Patrick Duncan	41,721

as its attorneys/agents with full power of substitution to prosecute this reissue application and to transact all business in the Patent and Trademark Office in connection therewith.

Please direct all correspondence regarding this application to the following:

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Attn: Mark C. Pickering
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San Francisco, CA 94111

Telephone: (415) 433-4150
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Date: 1-6-99

By: _____

Name: John M. Clark, III

Title: Sr. Vice President, General Counsel & Secretary

Express Mail Label No.:
EL151571733US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of	)	
	)	
Amos Intrater et al.	)	**DECLARATION OF AMOS INTRATER**
	)	
Patent No. 5,630,153	)	
	)	
Issued: May 13, 1997	)	2001 Ferry Building
	)	San Francisco, CA 94111
For: **INTEGRATED DIGITAL SIGNAL PROCESSOR/GENERAL PURPOSE CPU WITH SHARED INTERNAL MEMORY**	)	(415) 433-4150
	)	Attorney Docket No:
	)	NSC8-8400

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

I, Amos Intrater, hereby declare that:

1. This declaration is directed to U.S. Patent No. 5,630,153 (the '153 patent), which issued on May 13, 1997.

2. My residence and post office address are both 81 Emek Hefer St., Netanya, 42220 Israel. I am a citizen of Israel.

3. I am a joint inventor of the invention recited in the claims of the '153 patent. The names, addresses, and citizenships of my co-inventors are:

a. Gideon Intrater. The residence and post office address of Gideon Intrater are both 1035 Aster Ave., Sunnyvale, CA 94086. Gideon Intrater is an Israeli citizen.

b. Moshe Doron. The residence and post office address of Moshe Doron are both 7 Hashachar St., Raanana, 43564 Israel. Moshe Doron is an Israeli citizen.

c. Lev Epstein. The residence and post office address of Lev Epstein are both 13A Admonit St., Ramat Poleg, Netanya, Israel. Lev Epstein is an Israeli citizen.

d. Maurice Valentaten. The residence and post office address of Maurice Valentaten are both Kurt Huber Ring 3, 82256 Fuerstenfeldbruck, Germany. Maurice Valentaten is a Belgian citizen.

e. Israel Greiss. The residence and post office address of Israel Greiss are both 48 Rambam St., Raanana, 43602 Israel. Israel Greiss is an Israeli citizen.

4. I hereby state that I have reviewed and understand the contents of the specification of the '153 patent, including the claims, as amended by any amendments specifically referred to in this declaration.

5. I believe my co-inventors and I are the original and first inventors of the subject matter which is described and claimed in the '153 patent for which a reissue patent is sought.

6. I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37 of the Code of Federal Regulations (CFR) §1.56.

7. I hereby state that one error that is being relied upon as the basis for reissue is that claims 1, 9, and 10 of the '153 patent appear to read on page 12 and Chapter 13, titled TMS32020 and MC68000 Interface, by Charles Crowell, of Digital Signal

Processing Applications with the TMS320 Family, Volume I, Edited by Kun-Shan Lin, Ph.D., dated September 1986, which has not been previously considered by the Patent Office. Page 12 and the Crowell chapter of the Digital Signal Processing Applications (DSPA) document came to our attention after issuance of the '153 patent. A copy of page 12 and the Crowell chapter from the DSPA document are attached in an accompanying IDS.

Page 12 and the Crowell chapter from the DSPA document cited in the IDS are from a June 1989 reprint. I understand that the assignee of the '153 patent, National Semiconductor, has searched for the 1986 document, but has been unable to find it. Although page 12 and the Crowell chapter of the DSPA document cited in the IDS are from a June 1989 reprint, I believe that page 12 and the Crowell chapter of the June 1989 DSPA document are an exact copy of page 12 and the Crowell chapter of the September 1986 DSPA document because the June 1989 reprint was not separately copyrighted, and was printed with 1986 dates throughout the document. I do not believe that documents with a June 1989 publication date are prior art with respect to the '153 patent because my co-inventors and I have an earlier date of conception.

Since claims 1, 9, and 10 appear to read on page 12 and the Crowell chapter of the DSPA document, I believe the original patent to be wholly or partly inoperative or invalid by reason of my co-inventors and I claiming more than we had a right to claim.

Specifically, claim 1 of the '153 patent requires:

> "a shared bus for transferring both data and instructions; [and]

> "a shared memory array for storing both data and general purpose instructions and that is connected for transfer of both data and general purpose instructions between the shared bus and the shared memory array". [Brackets added].

In the schematic diagrams shown on pages 376-377, the Crowell document discloses an address bus A BUS and a data bus D BUS for transferring both data and instructions. In addition, on page 372, column 1, line 11, the Crowell document teaches that the IMS1421-40 chips are shared memories which, as shown on page 377, are connected to the shared bus (the address and data buses A BUS and D BUS). Further, on page 371, in the System Configuration section, Crowell discloses that the shared memories (the IMS1421-40 ships) store both data and instructions.

Claim 1 of the '153 patent also requires:

> "a digital signal execution unit connected to the shared bus for processing the digital signal utilizing both data transferred between the shared memory array and the digital signal execution unit on the shared bus and a selected sequence of individual digital signal processor (DSP) instructions, the selected sequence of DSP instructions consisting of individual general purpose instructions transferred between the shared memory array and the digital signal execution unit on the shared bus".

On page 373, under the Summary section, Crowell teaches that the TMS32020 chip is a digital signal processor (DSP) which, as shown on page 377, is connected to the shared memories (the IMS1421-40 chips) via the shared bus (the address and data buses A BUS and D BUS). Further, on page 371, in the System Configuration section, Crowell discloses that both instructions and data are transferred to the

shared memories (the IMS1421-40 chips) for use by the DSP (the TMS32020 chip).

Claim 1 of the '153 patent further requires:

> "a general purpose processor connected to the shared bus for controlling the digital signal execution unit by selecting each general purpose instruction to be transferred to the digital signal execution unit from the shared memory array,
>
> "whereby the selected sequence of individual DSP instructions executed by the digital signal execution unit is selectively configurable by the general purpose processor."

On page 371, in the Introduction section, Crowell discloses that the MC68000 chip is a host processor, while on page 372, column 1, line 9, Crowell teaches that the 74LS241 chips are buffers.

On pages 376-377, Crowell's schematic diagrams show that the address and data lines from the MC68000 processor are connected to the shared bus (the address and data buses A BUS and D BUS) via the buffers (the 74LS241 chips). Thus, when the 74LS241 buffers are turned on, the MC68000 processor is connected to the shared bus (the address and data buses A BUS and D BUS).

In addition, on page 371, in the System Configuration section, Crowell discloses that both instructions and data are transferred from the 68000 host processor to the shared memories (the IMS1421-40 chips), and then to the DSP (the TMS32020 chip). Thus, claim 1 of the '153 patent appears to read on the Crowell document.

With respect to independent claim 9 of the '153 patent, this claim requires:

> "(a) a digital signal execution unit that recovers digital data from the digital signal by

executing a selected sequence of digital signal processor (DSP) instructions;

(b) a general purpose processor that selects the sequence of DSP instructions for execution by the digital signal execution unit from a set of DSP instructions and that performs general purpose processing tasks by executing general purpose instructions utilizing selected data;

(c) a shared internal bus for transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected; and

(d) a shared internal memory array connected to the shared internal bus via an internal input/output port of the shared internal memory array such that the shared internal memory array is accessible by the digital signal execution unit via the internal input/output port for transferring operands utilizable by the digital signal execution unit between the shared internal memory array and the digital signal execution unit on the shared internal bus and such that the shared internal memory array is accessible by the general purpose processor via the internal input/output port for transferring the general purpose instructions and the selected data between the shared internal memory array and the general purpose processor on the shared internal bus;"

The above discussion with respect to the digital signal execution unit, the general purpose processor, the shared internal bus, and the shared internal memory array of claim 1 also apply to claim 9.

Claim 9 of the '153 patent further requires:

"wherein the digital signal execution unit includes an internal address generator for retrieving operands from the shared internal memory array via the shared internal bus for use by the digital signal execution unit in executing the selected sequence of DSP instructions."

On page 12 of the DSPA document, which shows the internal core of the TMS32020 chip, the registers

which are labeled ARO(16), AR1(16), AR2(16), AR3(16), and AR4(16) function as an internal address generator as required by claim 9. Thus, claim 9 of the '153 patent appears to read on page 12 and the Crowell chapter of the DSPA document.

With respect to independent claim 10 of the '153 patent, elements (a), (b), (c), and (d) are the same as the corresponding elements in claim 9. Thus, the above discussion with respect to the digital signal execution unit, the general purpose processor, the shared internal bus, and the shared internal memory array of claim 1 also apply to claim 10.

Claim 10 of the '153 patent further requires:

> "(e) an instruction sequencing unit connected to the shared internal bus for controlling the flow of execution of the DSP instructions and the general purpose instructions."

Although the Crowell document does not explicitly show this unit, it is believed that one skilled in the art would understand that the MC68000 chip has circuitry which performs this function. Thus, claim 10 of the '153 patent further appears to read on the Crowell document.

As a result, claims 1, 9, and 10 are cancelled in this reissue application.

8. I hereby further state that a second error that is being relied upon as a basis for reissue is that none of the claims in the '153 patent provide coverage of the scope provided by new reissue claims 11-44. As a result, I believe the original patent to be wholly or partly inoperative or invalid by reason of my co-inventors and I claiming less than we had a right to claim.

New independent reissue claims 11, 20, and 29 define the invention as follows:

> 11. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register and starting execution of an instruction in response to the GPP loading information into the register.

> 20. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register and executing an instruction in response to the GPP loading information into the register, the information loaded into the register identifying the instruction.

> 29. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register, executing an instruction in response to the GPP loading information into the register, and retrieving operands required by the instruction from the memory by processing the information loaded into the register.

Support for new claims 11, 20, and 29 may be found in FIG. 3, in column 6, lines 37-67, column 8, lines 25-53, and column 9, lines 55-65 of the '153 patent specification.

None of the existing claims provide a scope of coverage which is the same as, or comparable to, the

scope of coverage now provided by new reissue claims 11, 20, and 29. Independent claim 4 and dependent claims 5-6 are the only existing claims that recite a DSP which has a register (a control register). Claims 4-6, however, do not recite that the GPP loads operands into the memory.

In addition, none of the previously submitted claims provided a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 11, 20, and 29. The only previously submitted claims which recite a DSP that has a register are independent claim 10 and dependent claims 11-14 in the originally-filed application (Application Serial No. 07/467,148 filed on January 18, 1990).

Independent claim 10, in addition to reciting a register, also recited an internal memory that provided storage for data retrieved by the GPP. Originally-filed claim 10, however, further recited a number of elements which are not present in new reissue claims 11, 20, and 29; namely a bus interface unit and an external memory. Thus, originally-filed claims 10-14 did not provide a scope of coverage which is the same as, or comparable to, new reissue claims 11, 20, and 29.

Subsequently, originally-filed claim 10 was amended in a Preliminary Amendment filed on January 29, 1993 as part of an FWC application (Application Serial No. 08/011,102 filed on January 29, 1993). The amendment added limitations to originally-filed claim 10, and deleted the bus interface unit, the external memory, and reference to the internal memory providing storage for data retrieved by the GPP.

In addition, dependent claim 11 was also amended to add further limitations to the multiplier/

accumulator unit, while claims 13 and 14 were cancelled (dependent claim 12 further defines the address generator of original claim 10). Thus, claims 10-11, as amended, and claim 12 did not provide a scope of coverage which is the same as, or comparable to, new reissue claims 11, 20, and 29.

Following this, amended claim 10 was cancelled in favor of claim 27 in the Amendment filed on January 7, 1994. In addition, claims 11-12 were amended to further recite the multiply/accumulate unit, and the address generator. Claims 27 and 11-12, in turn, subsequently issued as claims 4-6, respectively, of the '153 patent.

Therefore, none of the existing claims, and none of the previously presented claims, provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 11, 20, and 29.

New dependent reissue claims 12-19, 21-28, and 30-36 further recite the invention as follows:

> 12. The data processing system of claim 11 wherein the operands held in the memory are randomly accessible.
>
> 13. The data processing system of claim 11 wherein the information placed in the register identifies the instruction to be executed.
>
> 14. The data processing system of claim 11 wherein the DSP is connected to the memory via a second bus.
>
> 15. The data processing system of claim 11 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.
>
> 16. The data processing system of claim 11 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

17. The data processing system of claim 11 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

18. The data processing system of claim 11 wherein the DSP only executes a single instruction when said information is loaded into the register.

19. The data processing system of claim 11 wherein the DSP retrieves the operands from the memory.

21. The data processing system of claim 20 wherein the operands held in the memory are randomly accessible.

22. The data processing system of claim 20 wherein the information placed in the register identifies the instruction to be executed.

23. The data processing system of claim 20 wherein the DSP is connected to the memory via a second bus.

24. The data processing system of claim 20 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

25. The data processing system of claim 20 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

26. The data processing system of claim 20 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

27. The data processing system of claim 20 wherein the DSP only executes a single instruction when said information is loaded into the register.

28. The data processing system of claim 20 wherein the DSP retrieves the operands from the memory.

30. The data processing system of claim 29 wherein the operands held in the memory are randomly accessible.

31. The data processing system of claim 29 wherein the information placed in the register identifies the instruction to be executed.

32. The data processing system of claim 29 wherein the DSP is connected to the memory via a second bus.

33. The data processing system of claim 29 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

34. The data processing system of claim 29 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

35. The data processing system of claim 29 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

36. The data processing system of claim 29 wherein the DSP only executes a single instruction when said information is loaded into the register.

Support for new reissue claims 12, 21, and 30 may be found in column 6, lines 5-7 of the '153 patent specification. Support for new reissue claims 13, 22, and 31 may be found in column 6, lines 47-50 and column 9, lines 55-57 of the '153 patent specification. Support for new reissue claims 14, 23, and 32 may be found in FIG. 3 of the '153 patent specification. Support for new reissue claims 15, 24, and 33 may be found in column 6, lines 50-53 of the '153 patent specification. Support for new reissue claims 16-18, 25-27, and 34-36 may be found in column 6, lines 54-67 of the '153 patent specification. Support for new reissue claims 19 and 28 may be found in column 6, lines 45-46.

Since existing claims 4-6 fail to recite that the GPP loads operands into the memory, none of the existing claims provide a scope of coverage which is

the same as, or comparable to, the scope of coverage now provided by new reissue claims 12-19, 21-28, and 30-36.

In addition, since originally-filed claims 10-14 recited elements which are not recited in new reissue claims 12-19, 21-28, and 30-36; and amended claims 10-11 and claim 12 no longer recite that the GPP loads operands into the memory, none of the previously submitted claims provided a scope of coverage which is the same as, or comparable to, new reissue claims 12-19, 21-28, and 30-36.

In addition, new independent reissue claim 37 recites the invention as follows:

> 37. A data processing system comprising:
> a digital signal processor (DSP) that processes digital data by executing an algorithm that includes a specific sequence of DSP operations;
> a general purpose processor (GPP) that selects the sequence of DSP operations for execution by the DSP from a basic set of DSP operations, and that performs general purpose tasks utilizing selected instructions and data;
> a bus to which both the DSP and the GPP are connected;
> a memory connected to the bus such that the memory is accessible by the DSP for retrieving operands utilized by the DSP in executing the selected sequence of DSP operations and by the GPP for loading operands required for execution of the selected DSP algorithm and/or instructions and data for use by the GPP for controlling the DSP; and
> a control register of the DSP characterized in that said GPP invokes a first DSP operation in the selected sequence by issuing a corresponding command directly to said control register of the DSP.

Support for new reissue claim 37 may be found in FIG. 3, and column 6, lines 37-67 of the '153 patent specification.

As with new reissue claims 11, 20, and 29, new reissue claim 37 recites that the GPP loads operands into the memory, and that the DSP has a register, but does not recite either a bus interface unit or an external memory. As a result, none of the existing claims, and none of the previously submitted claims, provide a scope of coverage which is the same as, or comparable to, the scope of coverage provide by new reissue claim 37.

New dependent reissue claims 38-39 further recite the invention as follows:

> 38. The system of claim 37 wherein the DSP, in response to receiving a first DSP operation, places the GPP in a continuous wait state while the DSP performs the first DSP operation utilizing operands retrieved from the memory.
>
> 39. The system of claim 37 wherein, upon completion of execution of the selected sequence of the DSP operations, the GPP downloads contents of the memory and retrieves a new set of operands, instructions, and data for a new sequence of DSP operations.

Support for claims 38-39 may be found in column 8, lines 37-67 of the '153 patent specification.

Since existing claims 4-6 fail to recite that the GPP loads operands into the memory, none of the existing claims provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 38-39.

In addition, since originally-filed claims 10-14 recited elements which are not recited in new reissue claims 38-39, and amended claims 10-11 and claim 12 no longer recite that the GPP loads operands into the memory, none of the previously submitted claims

provided a scope of coverage which is the same as, or comparable to, new reissue claims 38-39.

Further, new independent reissue claim 40 recites the invention as follows:

> 40. A data processing system comprising:
> a first data bus;
> a second data bus;
> a memory connected to the first data bus and the second data bus;
> a general purpose processor (GPP) connected to the first data bus, the GPP loading operands into the memory via the first data bus; and
> a digital signal processor (DSP) connected to the first data bus and the second data bus, the DSP executing an instruction identified by the GPP, and retrieving operands from the memory via the second data bus.

Support for new claim 40 may be found in FIG. 3, and in column 6, lines 37-67 of the '153 patent specification.

None of the existing claims provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claim 40 as none of the existing and previously submitted claims recite a first memory and a DSP that are connected to both a first data bus and a second data bus.

New dependent reissue claims 41-44 further recite the invention as follows:

> 41. The data processing system of claim 40 wherein the operands held in the memory are randomly accessible.
>
> 42. The data processing system of claim 40 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.
>
> 43. The data processing system of claim 40 wherein the GPP reads a value that results from

executing the instruction after the DSP completes execution of the instruction.

44. The data processing system of claim 40 and further comprising:
a bus interface unit connected to the first data bus; and
a third data bus connected to the bus interface unit.

Support for new reissue claims 41-44 may be found in FIG. 3 and column 6, lines 37-67 of the '153 patent specification.

Since none of the existing claims, and none of the previously presented claims, recite a first memory and a DSP that are connected to both a first data bus and a second data bus, none of the existing claims, and none of the previously presented claims provide the scope of coverage provided by new reissue claims 41-44.

9. All errors being corrected in this reissue application up to the time of filing this declaration arose without any deceptive intention on my part.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such

willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: 07/19/98

By: A. Intrater
Amos Intrater

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of	
Amos Intrater et al.	**DECLARATION OF MOSHE DORON**
Patent No. 5,630,153	
Issued: May 13, 1997	2001 Ferry Building San Francisco, CA 94111 (415) 433-4150
For: **INTEGRATED DIGITAL SIGNAL PROCESSOR/GENERAL PURPOSE CPU WITH SHARED INTERNAL MEMORY**	Attorney Docket No: NSC8-8400

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

I, Moshe Doron, hereby declare that:

1. This declaration is directed to U.S. Patent No. 5,630,153 (the '153 patent), which issued on May 13, 1997.

2. My residence and post office address are both 7 Hashachar St., Raanana, 43564 Israel. I am a citizen of Israel.

3. I am a joint inventor of the invention recited in the claims of the '153 patent. The names, addresses, and citizenships of my co-inventors are:

a. Gideon Intrater. The residence and post office address of Gideon Intrater are both 1035 Aster Ave., Sunnyvale, CA 94086. Gideon Intrater is an Israeli citizen.

b. Amos Intrater. The residence and post office address of Amos Intrater are both 81 Emek Hefer St., Netanya, 42220 Israel. Amos Intrater is an Israeli citizen.

c. Lev Epstein. The residence and post office address of Lev Epstein are both 13A Admonit St., Ramat Poleg, Netanya, Israel. Lev Epstein is an Israeli citizen.

d. Maurice Valentaten. The residence and post office address of Maurice Valentaten are both Kurt Huber Ring 3, 82256 Fuerstenfeldbruck, Germany. Maurice Valentaten is a Belgian citizen.

e. Israel Greiss. The residence and post office address of Israel Greiss are both 48 Rambam St., Raanana, 43602 Israel. Israel Greiss is an Israeli citizen.

4. I hereby state that I have reviewed and understand the contents of the specification of the '153 patent, including the claims, as amended by any amendments specifically referred to in this declaration.

5. I believe my co-inventors and I are the original and first inventors of the subject matter which is described and claimed in the '153 patent for which a reissue patent is sought.

6. I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37 of the Code of Federal Regulations (CFR) §1.56.

7. I hereby state that one error that is being relied upon as the basis for reissue is that claims 1, 9, and 10 of the '153 patent appear to read on page 12 and Chapter 13, titled TMS32020 and MC68000 Interface, by Charles Crowell, of Digital Signal

Processing Applications with the TMS320 Family, Volume I, Edited by Kun-Shan Lin, Ph.D., dated September 1986, which has not been previously considered by the Patent Office. Page 12 and the Crowell chapter of the Digital Signal Processing Applications (DSPA) document came to our attention after issuance of the '153 patent. A copy of page 12 and the Crowell chapter from the DSPA document are attached in an accompanying IDS.

Page 12 and the Crowell chapter from the DSPA document cited in the IDS are from a June 1989 reprint. I understand that the assignee of the '153 patent, National Semiconductor, has searched for the 1986 document, but has been unable to find it. Although page 12 and the Crowell chapter of the DSPA document cited in the IDS are from a June 1989 reprint, I believe that page 12 and the Crowell chapter of the June 1989 DSPA document are an exact copy of page 12 and the Crowell chapter of the September 1986 DSPA document because the June 1989 reprint was not separately copyrighted, and was printed with 1986 dates throughout the document. I do not believe that documents with a June 1989 publication date are prior art with respect to the '153 patent because my co-inventors and I have an earlier date of conception.

Since claims 1, 9, and 10 appear to read on page 12 and the Crowell chapter of the DSPA document, I believe the original patent to be wholly or partly inoperative or invalid by reason of my co-inventors and I claiming more than we had a right to claim.

Specifically, claim 1 of the '153 patent requires:

> "a shared bus for transferring both data and instructions; [and]

> "a shared memory array for storing both data and general purpose instructions and that is connected for transfer of both data and general purpose instructions between the shared bus and the shared memory array". [Brackets added].

In the schematic diagrams shown on pages 376-377, the Crowell document discloses an address bus A BUS and a data bus D BUS for transferring both data and instructions. In addition, on page 372, column 1, line 11, the Crowell document teaches that the IMS1421-40 chips are shared memories which, as shown on page 377, are connected to the shared bus (the address and data buses A BUS and D BUS). Further, on page 371, in the System Configuration section, Crowell discloses that the shared memories (the IMS1421-40 ships) store both data and instructions.

Claim 1 of the '153 patent also requires:

> "a digital signal execution unit connected to the shared bus for processing the digital signal utilizing both data transferred between the shared memory array and the digital signal execution unit on the shared bus and a selected sequence of individual digital signal processor (DSP) instructions, the selected sequence of DSP instructions consisting of individual general purpose instructions transferred between the shared memory array and the digital signal execution unit on the shared bus".

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shared memories (the IMS1421-40 chips) for use by the DSP (the TMS32020 chip).

Claim 1 of the '153 patent further requires:

> "a general purpose processor connected to the shared bus for controlling the digital signal execution unit by selecting each general purpose instruction to be transferred to the digital signal execution unit from the shared memory array,
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> "whereby the selected sequence of individual DSP instructions executed by the digital signal execution unit is selectively configurable by the general purpose processor."

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In addition, on page 371, in the System Configuration section, Crowell discloses that both instructions and data are transferred from the 68000 host processor to the shared memories (the IMS1421-40 chips), and then to the DSP (the TMS32020 chip). Thus, claim 1 of the '153 patent appears to read on the Crowell document.

With respect to independent claim 9 of the '153 patent, this claim requires:

> "(a) a digital signal execution unit that recovers digital data from the digital signal by

executing a selected sequence of digital signal processor (DSP) instructions;

(b) a general purpose processor that selects the sequence of DSP instructions for execution by the digital signal execution unit from a set of DSP instructions and that performs general purpose processing tasks by executing general purpose instructions utilizing selected data;

(c) a shared internal bus for transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected; and

(d) a shared internal memory array connected to the shared internal bus via an internal input/output port of the shared internal memory array such that the shared internal memory array is accessible by the digital signal execution unit via the internal input/output port for transferring operands utilizable by the digital signal execution unit between the shared internal memory array and the digital signal execution unit on the shared internal bus and such that the shared internal memory array is accessible by the general purpose processor via the internal input/output port for transferring the general purpose instructions and the selected data between the shared internal memory array and the general purpose processor on the shared internal bus;"

The above discussion with respect to the digital signal execution unit, the general purpose processor, the shared internal bus, and the shared internal memory array of claim 1 also apply to claim 9.

Claim 9 of the '153 patent further requires:

"wherein the digital signal execution unit includes an internal address generator for retrieving operands from the shared internal memory array via the shared internal bus for use by the digital signal execution unit in executing the selected sequence of DSP instructions."

On page 12 of the DSPA document, which shows the internal core of the TMS32020 chip, the registers

which are labeled ARO(16), AR1(16), AR2(16), AR3(16), and AR4(16) function as an internal address generator as required by claim 9. Thus, claim 9 of the '153 patent appears to read on page 12 and the Crowell chapter of the DSPA document.

With respect to independent claim 10 of the '153 patent, elements (a), (b), (c), and (d) are the same as the corresponding elements in claim 9. Thus, the above discussion with respect to the digital signal execution unit, the general purpose processor, the shared internal bus, and the shared internal memory array of claim 1 also apply to claim 10.

Claim 10 of the '153 patent further requires:

> "(e) an instruction sequencing unit connected to the shared internal bus for controlling the flow of execution of the DSP instructions and the general purpose instructions."

Although the Crowell document does not explicitly show this unit, it is believed that one skilled in the art would understand that the MC68000 chip has circuitry which performs this function. Thus, claim 10 of the '153 patent further appears to read on the Crowell document.

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> a digital signal processor (DSP) connected to the first bus, the DSP having a register and starting execution of an instruction in response to the GPP loading information into the register.

> 20. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register and executing an instruction in response to the GPP loading information into the register, the information loaded into the register identifying the instruction.

> 29. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register, executing an instruction in response to the GPP loading information into the register, and retrieving operands required by the instruction from the memory by processing the information loaded into the register.

Support for new claims 11, 20, and 29 may be found in FIG. 3, in column 6, lines 37-67, column 8, lines 25-53, and column 9, lines 55-65 of the '153 patent specification.

None of the existing claims provide a scope of coverage which is the same as, or comparable to, the

scope of coverage now provided by new reissue claims 11, 20, and 29. Independent claim 4 and dependent claims 5-6 are the only existing claims that recite a DSP which has a register (a control register). Claims 4-6, however, do not recite that the GPP loads operands into the memory.

In addition, none of the previously submitted claims provided a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 11, 20, and 29. The only previously submitted claims which recite a DSP that has a register are independent claim 10 and dependent claims 11-14 in the originally-filed application (Application Serial No. 07/467,148 filed on January 18, 1990).

Independent claim 10, in addition to reciting a register, also recited an internal memory that provided storage for data retrieved by the GPP. Originally-filed claim 10, however, further recited a number of elements which are not present in new reissue claims 11, 20, and 29; namely a bus interface unit and an external memory. Thus, originally-filed claims 10-14 did not provide a scope of coverage which is the same as, or comparable to, new reissue claims 11, 20, and 29.

Subsequently, originally-filed claim 10 was amended in a Preliminary Amendment filed on January 29, 1993 as part of an FWC application (Application Serial No. 08/011,102 filed on January 29, 1993). The amendment added limitations to originally-filed claim 10, and deleted the bus interface unit, the external memory, and reference to the internal memory providing storage for data retrieved by the GPP.

In addition, dependent claim 11 was also amended to add further limitations to the multiplier/

accumulator unit, while claims 13 and 14 were cancelled (dependent claim 12 further defines the address generator of original claim 10). Thus, claims 10-11, as amended, and claim 12 did not provide a scope of coverage which is the same as, or comparable to, new reissue claims 11, 20, and 29.

Following this, amended claim 10 was cancelled in favor of claim 27 in the Amendment filed on January 7, 1994. In addition, claims 11-12 were amended to further recite the multiply/accumulate unit, and the address generator. Claims 27 and 11-12, in turn, subsequently issued as claims 4-6, respectively, of the '153 patent.

Therefore, none of the existing claims, and none of the previously presented claims, provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 11, 20, and 29.

New dependent reissue claims 12-19, 21-28, and 30-36 further recite the invention as follows:

> 12. The data processing system of claim 11 wherein the operands held in the memory are randomly accessible.
>
> 13. The data processing system of claim 11 wherein the information placed in the register identifies the instruction to be executed.
>
> 14. The data processing system of claim 11 wherein the DSP is connected to the memory via a second bus.
>
> 15. The data processing system of claim 11 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.
>
> 16. The data processing system of claim 11 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

17. The data processing system of claim 11 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

18. The data processing system of claim 11 wherein the DSP only executes a single instruction when said information is loaded into the register.

19. The data processing system of claim 11 wherein the DSP retrieves the operands from the memory.

21. The data processing system of claim 20 wherein the operands held in the memory are randomly accessible.

22. The data processing system of claim 20 wherein the information placed in the register identifies the instruction to be executed.

23. The data processing system of claim 20 wherein the DSP is connected to the memory via a second bus.

24. The data processing system of claim 20 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

25. The data processing system of claim 20 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

26. The data processing system of claim 20 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

27. The data processing system of claim 20 wherein the DSP only executes a single instruction when said information is loaded into the register.

28. The data processing system of claim 20 wherein the DSP retrieves the operands from the memory.

30. The data processing system of claim 29 wherein the operands held in the memory are randomly accessible.

31. The data processing system of claim 29 wherein the information placed in the register identifies the instruction to be executed.

32. The data processing system of claim 29 wherein the DSP is connected to the memory via a second bus.

33. The data processing system of claim 29 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

34. The data processing system of claim 29 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

35. The data processing system of claim 29 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

36. The data processing system of claim 29 wherein the DSP only executes a single instruction when said information is loaded into the register.

Support for new reissue claims 12, 21, and 30 may be found in column 6, lines 5-7 of the '153 patent specification. Support for new reissue claims 13, 22, and 31 may be found in column 6, lines 47-50 and column 9, lines 55-57 of the '153 patent specification. Support for new reissue claims 14, 23, and 32 may be found in FIG. 3 of the '153 patent specification. Support for new reissue claims 15, 24, and 33 may be found in column 6, lines 50-53 of the '153 patent specification. Support for new reissue claims 16-18, 25-27, and 34-36 may be found in column 6, lines 54-67 of the '153 patent specification. Support for new reissue claims 19 and 28 may be found in column 6, lines 45-46.

Since existing claims 4-6 fail to recite that the GPP loads operands into the memory, none of the existing claims provide a scope of coverage which is

the same as, or comparable to, the scope of coverage now provided by new reissue claims 12-19, 21-28, and 30-36.

In addition, since originally-filed claims 10-14 recited elements which are not recited in new reissue claims 12-19, 21-28, and 30-36; and amended claims 10-11 and claim 12 no longer recite that the GPP loads operands into the memory, none of the previously submitted claims provided a scope of coverage which is the same as, or comparable to, new reissue claims 12-19, 21-28, and 30-36.

In addition, new independent reissue claim 37 recites the invention as follows:

> 37. A data processing system comprising:
> a digital signal processor (DSP) that processes digital data by executing an algorithm that includes a specific sequence of DSP operations;
> a general purpose processor (GPP) that selects the sequence of DSP operations for execution by the DSP from a basic set of DSP operations, and that performs general purpose tasks utilizing selected instructions and data;
> a bus to which both the DSP and the GPP are connected;
> a memory connected to the bus such that the memory is accessible by the DSP for retrieving operands utilized by the DSP in executing the selected sequence of DSP operations and by the GPP for loading operands required for execution of the selected DSP algorithm and/or instructions and data for use by the GPP for controlling the DSP; and
> a control register of the DSP characterized in that said GPP invokes a first DSP operation in the selected sequence by issuing a corresponding command directly to said control register of the DSP.

Support for new reissue claim 37 may be found in FIG. 3, and column 6, lines 37-67 of the '153 patent specification.

As with new reissue claims 11, 20, and 29, new reissue claim 37 recites that the GPP loads operands into the memory, and that the DSP has a register, but does not recite either a bus interface unit or an external memory. As a result, none of the existing claims, and none of the previously submitted claims, provide a scope of coverage which is the same as, or comparable to, the scope of coverage provide by new reissue claim 37.

New dependent reissue claims 38-39 further recite the invention as follows:

> 38. The system of claim 37 wherein the DSP, in response to receiving a first DSP operation, places the GPP in a continuous wait state while the DSP performs the first DSP operation utilizing operands retrieved from the memory.
>
> 39. The system of claim 37 wherein, upon completion of execution of the selected sequence of the DSP operations, the GPP downloads contents of the memory and retrieves a new set of operands, instructions, and data for a new sequence of DSP operations.

Support for claims 38-39 may be found in column 8, lines 37-67 of the '153 patent specification.

Since existing claims 4-6 fail to recite that the GPP loads operands into the memory, none of the existing claims provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 38-39.

In addition, since originally-filed claims 10-14 recited elements which are not recited in new reissue claims 38-39, and amended claims 10-11 and claim 12 no longer recite that the GPP loads operands into the memory, none of the previously submitted claims

provided a scope of coverage which is the same as, or comparable to, new reissue claims 38-39.

Further, new independent reissue claim 40 recites the invention as follows:

> 40. A data processing system comprising:
> a first data bus;
> a second data bus;
> a memory connected to the first data bus and the second data bus;
> a general purpose processor (GPP) connected to the first data bus, the GPP loading operands into the memory via the first data bus; and
> a digital signal processor (DSP) connected to the first data bus and the second data bus, the DSP executing an instruction identified by the GPP, and retrieving operands from the memory via the second data bus.

Support for new claim 40 may be found in FIG. 3, and in column 6, lines 37-67 of the '153 patent specification.

None of the existing claims provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claim 40 as none of the existing and previously submitted claims recite a first memory and a DSP that are connected to both a first data bus and a second data bus.

New dependent reissue claims 41-44 further recite the invention as follows:

> 41. The data processing system of claim 40 wherein the operands held in the memory are randomly accessible.
>
> 42. The data processing system of claim 40 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.
>
> 43. The data processing system of claim 40 wherein the GPP reads a value that results from

executing the instruction after the DSP completes execution of the instruction.

44. The data processing system of claim 40 and further comprising:
a bus interface unit connected to the first data bus; and
a third data bus connected to the bus interface unit.

Support for new reissue claims 41-44 may be found in FIG. 3 and column 6, lines 37-67 of the '153 patent specification.

Since none of the existing claims, and none of the previously presented claims, recite a first memory and a DSP that are connected to both a first data bus and a second data bus, none of the existing claims, and none of the previously presented claims provide the scope of coverage provided by new reissue claims 41-44.

9. All errors being corrected in this reissue application up to the time of filing this declaration arose without any deceptive intention on my part.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such

willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: July 12, 1998 By: ________________
Moshe Doron

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of	
Amos Intrater et al.	**DECLARATION OF GIDEON INTRATER**
Patent No. 5,630,153	
Issued: May 13, 1997	2001 Ferry Building San Francisco, CA 94111
For: **INTEGRATED DIGITAL SIGNAL PROCESSOR/GENERAL PURPOSE CPU WITH SHARED INTERNAL MEMORY**	(415) 433-4150 Attorney Docket No: NSC8-8400

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

I, Gideon Intrater, hereby declare that:

1. This declaration is directed to U.S. Patent No. 5,630,153 (the '153 patent), which issued on May 13, 1997.

2. My residence and post office address are both 1035 Aster Ave., Sunnyvale, CA 94086. I am a citizen of Israel.

3. I am a joint inventor of the invention recited in the claims of the '153 patent. The names, addresses, and citizenships of my co-inventors are:

a. Amos Intrater. The residence and post office address of Amos Intrater are both 81 Emek Hefer St., Netanya, 42220 Israel. Amos Intrater is an Israeli citizen.

b. Moshe Doron. The residence and post office address of Moshe Doron are both 7 Hashachar St., Raanana, 43564 Israel. Moshe Doron is an Israeli citizen.

c. Lev Epstein. The residence and post office address of Lev Epstein are both 13A Admonit St., Ramat Poleg, Netanya, Israel. Lev Epstein is an Israeli citizen.

d. Maurice Valentaten. The residence and post office address of Maurice Valentaten are both Kurt Huber Ring 3, 82256 Fuerstenfeldbruck, Germany. Maurice Valentaten is a Belgian citizen.

e. Israel Greiss. The residence and post office address of Israel Greiss are both 48 Rambam St., Raanana, 43602 Israel. Israel Greiss is an Israeli citizen.

4. I hereby state that I have reviewed and understand the contents of the specification of the '153 patent, including the claims, as amended by any amendments specifically referred to in this declaration.

5. I believe my co-inventors and I are the original and first inventors of the subject matter which is described and claimed in the '153 patent for which a reissue patent is sought.

6. I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37 of the Code of Federal Regulations (CFR) §1.56.

7. I hereby state that one error that is being relied upon as the basis for reissue is that claims 1, 9, and 10 of the '153 patent appear to read on page 12 and Chapter 13, titled TMS32020 and MC68000 Interface, by Charles Crowell, of Digital Signal

Processing Applications with the TMS320 Family, Volume I, Edited by Kun-Shan Lin, Ph.D., dated September 1986, which has not been previously considered by the Patent Office. Page 12 and the Crowell chapter of the Digital Signal Processing Applications (DSPA) document came to our attention after issuance of the '153 patent. A copy of page 12 and the Crowell chapter from the DSPA document are attached in an accompanying IDS.

Page 12 and the Crowell chapter from the DSPA document cited in the IDS are from a June 1989 reprint. I understand that the assignee of the '153 patent, National Semiconductor, has searched for the 1986 document, but has been unable to find it. Although page 12 and the Crowell chapter of the DSPA document cited in the IDS are from a June 1989 reprint, I believe that page 12 and the Crowell chapter of the June 1989 DSPA document are an exact copy of page 12 and the Crowell chapter of the September 1986 DSPA document because the June 1989 reprint was not separately copyrighted, and was printed with 1986 dates throughout the document. I do not believe that documents with a June 1989 publication date are prior art with respect to the '153 patent because my co-inventors and I have an earlier date of conception.

Since claims 1, 9, and 10 appear to read on page 12 and the Crowell chapter of the DSPA document, I believe the original patent to be wholly or partly inoperative or invalid by reason of my co-inventors and I claiming more than we had a right to claim.

Specifically, claim 1 of the '153 patent requires:

> "a shared bus for transferring both data and instructions; [and]

> "a shared memory array for storing both data and general purpose instructions and that is connected for transfer of both data and general purpose instructions between the shared bus and the shared memory array". [Brackets added].

In the schematic diagrams shown on pages 376-377, the Crowell document discloses an address bus A BUS and a data bus D BUS for transferring both data and instructions. In addition, on page 372, column 1, line 11, the Crowell document teaches that the IMS1421-40 chips are shared memories which, as shown on page 377, are connected to the shared bus (the address and data buses A BUS and D BUS). Further, on page 371, in the System Configuration section, Crowell discloses that the shared memories (the IMS1421-40 ships) store both data and instructions.

Claim 1 of the '153 patent also requires:

> "a digital signal execution unit connected to the shared bus for processing the digital signal utilizing both data transferred between the shared memory array and the digital signal execution unit on the shared bus and a selected sequence of individual digital signal processor (DSP) instructions, the selected sequence of DSP instructions consisting of individual general purpose instructions transferred between the shared memory array and the digital signal execution unit on the shared bus".

On page 373, under the Summary section, Crowell teaches that the TMS32020 chip is a digital signal processor (DSP) which, as shown on page 377, is connected to the shared memories (the IMS1421-40 chips) via the shared bus (the address and data buses A BUS and D BUS). Further, on page 371, in the System Configuration section, Crowell discloses that both instructions and data are transferred to the

shared memories (the IMS1421-40 chips) for use by the DSP (the TMS32020 chip).

Claim 1 of the '153 patent further requires:

> "a general purpose processor connected to the shared bus for controlling the digital signal execution unit by selecting each general purpose instruction to be transferred to the digital signal execution unit from the shared memory array,
>
> "whereby the selected sequence of individual DSP instructions executed by the digital signal execution unit is selectively configurable by the general purpose processor."

On page 371, in the Introduction section, Crowell discloses that the MC68000 chip is a host processor, while on page 372, column 1, line 9, Crowell teaches that the 74LS241 chips are buffers.

On pages 376-377, Crowell's schematic diagrams show that the address and data lines from the MC68000 processor are connected to the shared bus (the address and data buses A BUS and D BUS) via the buffers (the 74LS241 chips). Thus, when the 74LS241 buffers are turned on, the MC68000 processor is connected to the shared bus (the address and data buses A BUS and D BUS).

In addition, on page 371, in the System Configuration section, Crowell discloses that both instructions and data are transferred from the 68000 host processor to the shared memories (the IMS1421-40 chips), and then to the DSP (the TMS32020 chip). Thus, claim 1 of the '153 patent appears to read on the Crowell document.

With respect to independent claim 9 of the '153 patent, this claim requires:

> "(a) a digital signal execution unit that recovers digital data from the digital signal by

executing a selected sequence of digital signal processor (DSP) instructions;

(b) a general purpose processor that selects the sequence of DSP instructions for execution by the digital signal execution unit from a set of DSP instructions and that performs general purpose processing tasks by executing general purpose instructions utilizing selected data;

(c) a shared internal bus for transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected; and

(d) a shared internal memory array connected to the shared internal bus via an internal input/output port of the shared internal memory array such that the shared internal memory array is accessible by the digital signal execution unit via the internal input/output port for transferring operands utilizable by the digital signal execution unit between the shared internal memory array and the digital signal execution unit on the shared internal bus and such that the shared internal memory array is accessible by the general purpose processor via the internal input/output port for transferring the general purpose instructions and the selected data between the shared internal memory array and the general purpose processor on the shared internal bus;"

The above discussion with respect to the digital signal execution unit, the general purpose processor, the shared internal bus, and the shared internal memory array of claim 1 also apply to claim 9.

Claim 9 of the '153 patent further requires:

"wherein the digital signal execution unit includes an internal address generator for retrieving operands from the shared internal memory array via the shared internal bus for use by the digital signal execution unit in executing the selected sequence of DSP instructions."

On page 12 of the DSPA document, which shows the internal core of the TMS32020 chip, the registers

which are labeled ARO(16), AR1(16), AR2(16), AR3(16), and AR4(16) function as an internal address generator as required by claim 9. Thus, claim 9 of the '153 patent appears to read on page 12 and the Crowell chapter of the DSPA document.

With respect to independent claim 10 of the '153 patent, elements (a), (b), (c), and (d) are the same as the corresponding elements in claim 9. Thus, the above discussion with respect to the digital signal execution unit, the general purpose processor, the shared internal bus, and the shared internal memory array of claim 1 also apply to claim 10.

Claim 10 of the '153 patent further requires:

> "(e) an instruction sequencing unit connected to the shared internal bus for controlling the flow of execution of the DSP instructions and the general purpose instructions."

Although the Crowell document does not explicitly show this unit, it is believed that one skilled in the art would understand that the MC68000 chip has circuitry which performs this function. Thus, claim 10 of the '153 patent further appears to read on the Crowell document.

As a result, claims 1, 9, and 10 are cancelled in this reissue application.

8. I hereby further state that a second error that is being relied upon as a basis for reissue is that none of the claims in the '153 patent provide coverage of the scope provided by new reissue claims 11-44. As a result, I believe the original patent to be wholly or partly inoperative or invalid by reason of my co-inventors and I claiming less than we had a right to claim.

New independent reissue claims 11, 20, and 29 define the invention as follows:

> 11. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register and starting execution of an instruction in response to the GPP loading information into the register.

> 20. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register and executing an instruction in response to the GPP loading information into the register, the information loaded into the register identifying the instruction.

> 29. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register, executing an instruction in response to the GPP loading information into the register, and retrieving operands required by the instruction from the memory by processing the information loaded into the register.

Support for new claims 11, 20, and 29 may be found in FIG. 3, in column 6, lines 37-67, column 8, lines 25-53, and column 9, lines 55-65 of the '153 patent specification.

None of the existing claims provide a scope of coverage which is the same as, or comparable to, the

scope of coverage now provided by new reissue claims 11, 20, and 29. Independent claim 4 and dependent claims 5-6 are the only existing claims that recite a DSP which has a register (a control register). Claims 4-6, however, do not recite that the GPP loads operands into the memory.

In addition, none of the previously submitted claims provided a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 11, 20, and 29. The only previously submitted claims which recite a DSP that has a register are independent claim 10 and dependent claims 11-14 in the originally-filed application (Application Serial No. 07/467,148 filed on January 18, 1990).

Independent claim 10, in addition to reciting a register, also recited an internal memory that provided storage for data retrieved by the GPP. Originally-filed claim 10, however, further recited a number of elements which are not present in new reissue claims 11, 20, and 29; namely a bus interface unit and an external memory. Thus, originally-filed claims 10-14 did not provide a scope of coverage which is the same as, or comparable to, new reissue claims 11, 20, and 29.

Subsequently, originally-filed claim 10 was amended in a Preliminary Amendment filed on January 29, 1993 as part of an FWC application (Application Serial No. 08/011,102 filed on January 29, 1993). The amendment added limitations to originally-filed claim 10, and deleted the bus interface unit, the external memory, and reference to the internal memory providing storage for data retrieved by the GPP.

In addition, dependent claim 11 was also amended to add further limitations to the multiplier/

accumulator unit, while claims 13 and 14 were cancelled (dependent claim 12 further defines the address generator of original claim 10). Thus, claims 10-11, as amended, and claim 12 did not provide a scope of coverage which is the same as, or comparable to, new reissue claims 11, 20, and 29.

Following this, amended claim 10 was cancelled in favor of claim 27 in the Amendment filed on January 7, 1994. In addition, claims 11-12 were amended to further recite the multiply/accumulate unit, and the address generator. Claims 27 and 11-12, in turn, subsequently issued as claims 4-6, respectively, of the '153 patent.

Therefore, none of the existing claims, and none of the previously presented claims, provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 11, 20, and 29.

New dependent reissue claims 12-19, 21-28, and 30-36 further recite the invention as follows:

> 12. The data processing system of claim 11 wherein the operands held in the memory are randomly accessible.
>
> 13. The data processing system of claim 11 wherein the information placed in the register identifies the instruction to be executed.
>
> 14. The data processing system of claim 11 wherein the DSP is connected to the memory via a second bus.
>
> 15. The data processing system of claim 11 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.
>
> 16. The data processing system of claim 11 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

17. The data processing system of claim 11 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

18. The data processing system of claim 11 wherein the DSP only executes a single instruction when said information is loaded into the register.

19. The data processing system of claim 11 wherein the DSP retrieves the operands from the memory.

21. The data processing system of claim 20 wherein the operands held in the memory are randomly accessible.

22. The data processing system of claim 20 wherein the information placed in the register identifies the instruction to be executed.

23. The data processing system of claim 20 wherein the DSP is connected to the memory via a second bus.

24. The data processing system of claim 20 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

25. The data processing system of claim 20 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

26. The data processing system of claim 20 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

27. The data processing system of claim 20 wherein the DSP only executes a single instruction when said information is loaded into the register.

28. The data processing system of claim 20 wherein the DSP retrieves the operands from the memory.

30. The data processing system of claim 29 wherein the operands held in the memory are randomly accessible.

31. The data processing system of claim 29 wherein the information placed in the register identifies the instruction to be executed.

32. The data processing system of claim 29 wherein the DSP is connected to the memory via a second bus.

33. The data processing system of claim 29 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

34. The data processing system of claim 29 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

35. The data processing system of claim 29 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

36. The data processing system of claim 29 wherein the DSP only executes a single instruction when said information is loaded into the register.

Support for new reissue claims 12, 21, and 30 may be found in column 6, lines 5-7 of the '153 patent specification. Support for new reissue claims 13, 22, and 31 may be found in column 6, lines 47-50 and column 9, lines 55-57 of the '153 patent specification. Support for new reissue claims 14, 23, and 32 may be found in FIG. 3 of the '153 patent specification. Support for new reissue claims 15, 24, and 33 may be found in column 6, lines 50-53 of the '153 patent specification. Support for new reissue claims 16-18, 25-27, and 34-36 may be found in column 6, lines 54-67 of the '153 patent specification. Support for new reissue claims 19 and 28 may be found in column 6, lines 45-46.

Since existing claims 4-6 fail to recite that the GPP loads operands into the memory, none of the existing claims provide a scope of coverage which is

the same as, or comparable to, the scope of coverage now provided by new reissue claims 12-19, 21-28, and 30-36.

In addition, since originally-filed claims 10-14 recited elements which are not recited in new reissue claims 12-19, 21-28, and 30-36; and amended claims 10-11 and claim 12 no longer recite that the GPP loads operands into the memory, none of the previously submitted claims provided a scope of coverage which is the same as, or comparable to, new reissue claims 12-19, 21-28, and 30-36.

In addition, new independent reissue claim 37 recites the invention as follows:

> 37. A data processing system comprising:
> a digital signal processor (DSP) that processes digital data by executing an algorithm that includes a specific sequence of DSP operations;
> a general purpose processor (GPP) that selects the sequence of DSP operations for execution by the DSP from a basic set of DSP operations, and that performs general purpose tasks utilizing selected instructions and data;
> a bus to which both the DSP and the GPP are connected;
> a memory connected to the bus such that the memory is accessible by the DSP for retrieving operands utilized by the DSP in executing the selected sequence of DSP operations and by the GPP for loading operands required for execution of the selected DSP algorithm and/or instructions and data for use by the GPP for controlling the DSP; and
> a control register of the DSP characterized in that said GPP invokes a first DSP operation in the selected sequence by issuing a corresponding command directly to said control register of the DSP.

Support for new reissue claim 37 may be found in FIG. 3, and column 6, lines 37-67 of the '153 patent specification.

As with new reissue claims 11, 20, and 29, new reissue claim 37 recites that the GPP loads operands into the memory, and that the DSP has a register, but does not recite either a bus interface unit or an external memory. As a result, none of the existing claims, and none of the previously submitted claims, provide a scope of coverage which is the same as, or comparable to, the scope of coverage provide by new reissue claim 37.

New dependent reissue claims 38-39 further recite the invention as follows:

> 38. The system of claim 37 wherein the DSP, in response to receiving a first DSP operation, places the GPP in a continuous wait state while the DSP performs the first DSP operation utilizing operands retrieved from the memory.
>
> 39. The system of claim 37 wherein, upon completion of execution of the selected sequence of the DSP operations, the GPP downloads contents of the memory and retrieves a new set of operands, instructions, and data for a new sequence of DSP operations.

Support for claims 38-39 may be found in column 8, lines 37-67 of the '153 patent specification.

Since existing claims 4-6 fail to recite that the GPP loads operands into the memory, none of the existing claims provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 38-39.

In addition, since originally-filed claims 10-14 recited elements which are not recited in new reissue claims 38-39, and amended claims 10-11 and claim 12 no longer recite that the GPP loads operands into the memory, none of the previously submitted claims

provided a scope of coverage which is the same as, or comparable to, new reissue claims 38-39.

Further, new independent reissue claim 40 recites the invention as follows:

> 40. A data processing system comprising:
> a first data bus;
> a second data bus;
> a memory connected to the first data bus and the second data bus;
> a general purpose processor (GPP) connected to the first data bus, the GPP loading operands into the memory via the first data bus; and
> a digital signal processor (DSP) connected to the first data bus and the second data bus, the DSP executing an instruction identified by the GPP, and retrieving operands from the memory via the second data bus.

Support for new claim 40 may be found in FIG. 3, and in column 6, lines 37-67 of the '153 patent specification.

None of the existing claims provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claim 40 as none of the existing and previously submitted claims recite a first memory and a DSP that are connected to both a first data bus and a second data bus.

New dependent reissue claims 41-44 further recite the invention as follows:

> 41. The data processing system of claim 40 wherein the operands held in the memory are randomly accessible.
>
> 42. The data processing system of claim 40 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.
>
> 43. The data processing system of claim 40 wherein the GPP reads a value that results from

executing the instruction after the DSP completes execution of the instruction.

44. The data processing system of claim 40 and further comprising:

a bus interface unit connected to the first data bus; and

a third data bus connected to the bus interface unit.

Support for new reissue claims 41-44 may be found in FIG. 3 and column 6, lines 37-67 of the '153 patent specification.

Since none of the existing claims, and none of the previously presented claims, recite a first memory and a DSP that are connected to both a first data bus and a second data bus, none of the existing claims, and none of the previously presented claims provide the scope of coverage provided by new reissue claims 41-44.

9. All errors being corrected in this reissue application up to the time of filing this declaration arose without any deceptive intention on my part.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such

willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: 7/3/98 By: [signature]
Gideon Intrater

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of	
Amos Intrater et al.	**DECLARATION OF LEV EPSTEIN**
Patent No. 5,630,153	
Issued: May 13, 1997	2001 Ferry Building San Francisco, CA 94111
For: **INTEGRATED DIGITAL SIGNAL PROCESSOR/GENERAL PURPOSE CPU WITH SHARED INTERNAL MEMORY**	(415) 433-4150 Attorney Docket No: NSC8-8400

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

I, Lev Epstein, hereby declare that:

1. This declaration is directed to U.S. Patent No. 5,630,153 (the '153 patent), which issued on May 13, 1997.

2. My residence and post office address are both 13A Admonit St., Ramat Poleg, Netanya, Israel. I am a citizen of Israel.

3. I am a joint inventor of the invention recited in the claims of the '153 patent. The names, addresses, and citizenships of my co-inventors are:

a. Gideon Intrater. The residence and post office address of Gideon Intrater are both 1035 Aster Ave., Sunnyvale, CA 94086. Gideon Intrater is an Israeli citizen.

b. Amos Intrater. The residence and post office address of Amos Intrater are both 81 Emek Hefer St., Netanya, 42220 Israel. Amos Intrater is an Israeli citizen.

c. Moshe Doron. The residence and post office address of Moshe Doron are both 7 Hashachar St., Raanana, 43564 Israel. Moshe Doron is an Israeli citizen.

d. Maurice Valentaten. The residence and post office address of Maurice Valentaten are both Kurt Huber Ring 3, 82256 Fuerstenfeldbruck, Germany. Maurice Valentaten is a Belgian citizen.

e. Israel Greiss. The residence and post office address of Israel Greiss are both 48 Rambam St., Raanana, 43602 Israel. Israel Greiss is an Israeli citizen.

4. I hereby state that I have reviewed and understand the contents of the specification of the '153 patent, including the claims, as amended by any amendments specifically referred to in this declaration.

5. I believe my co-inventors and I are the original and first inventors of the subject matter which is described and claimed in the '153 patent for which a reissue patent is sought.

6. I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37 of the Code of Federal Regulations (CFR) §1.56.

7. I hereby state that one error that is being relied upon as the basis for reissue is that claims 1, 9, and 10 of the '153 patent appear to read on page 12 and Chapter 13, titled TMS32020 and MC68000 Interface, by Charles Crowell, of Digital Signal

Processing Applications with the TMS320 Family, Volume I, Edited by Kun-Shan Lin, Ph.D., dated September 1986, which has not been previously considered by the Patent Office. Page 12 and the Crowell chapter of the Digital Signal Processing Applications (DSPA) document came to our attention after issuance of the '153 patent. A copy of page 12 and the Crowell chapter from the DSPA document are attached in an accompanying IDS.

Page 12 and the Crowell chapter from the DSPA document cited in the IDS are from a June 1989 reprint. I understand that the assignee of the '153 patent, National Semiconductor, has searched for the 1986 document, but has been unable to find it. Although page 12 and the Crowell chapter of the DSPA document cited in the IDS are from a June 1989 reprint, I believe that page 12 and the Crowell chapter of the June 1989 DSPA document are an exact copy of page 12 and the Crowell chapter of the September 1986 DSPA document because the June 1989 reprint was not separately copyrighted, and was printed with 1986 dates throughout the document. I do not believe that documents with a June 1989 publication date are prior art with respect to the '153 patent because my co-inventors and I have an earlier date of conception.

Since claims 1, 9, and 10 appear to read on page 12 and the Crowell chapter of the DSPA document, I believe the original patent to be wholly or partly inoperative or invalid by reason of my co-inventors and I claiming more than we had a right to claim.

Specifically, claim 1 of the '153 patent requires:

> "a shared bus for transferring both data and instructions; [and]

> "a shared memory array for storing both data and general purpose instructions and that is connected for transfer of both data and general purpose instructions between the shared bus and the shared memory array". [Brackets added].

In the schematic diagrams shown on pages 376-377, the Crowell document discloses an address bus A BUS and a data bus D BUS for transferring both data and instructions. In addition, on page 372, column 1, line 11, the Crowell document teaches that the IMS1421-40 chips are shared memories which, as shown on page 377, are connected to the shared bus (the address and data buses A BUS and D BUS). Further, on page 371, in the System Configuration section, Crowell discloses that the shared memories (the IMS1421-40 ships) store both data and instructions.

Claim 1 of the '153 patent also requires:

> "a digital signal execution unit connected to the shared bus for processing the digital signal utilizing both data transferred between the shared memory array and the digital signal execution unit on the shared bus and a selected sequence of individual digital signal processor (DSP) instructions, the selected sequence of DSP instructions consisting of individual general purpose instructions transferred between the shared memory array and the digital signal execution unit on the shared bus".

On page 373, under the Summary section, Crowell teaches that the TMS32020 chip is a digital signal processor (DSP) which, as shown on page 377, is connected to the shared memories (the IMS1421-40 chips) via the shared bus (the address and data buses A BUS and D BUS). Further, on page 371, in the System Configuration section, Crowell discloses that both instructions and data are transferred to the

shared memories (the IMS1421-40 chips) for use by the DSP (the TMS32020 chip).

Claim 1 of the '153 patent further requires:

> "a general purpose processor connected to the shared bus for controlling the digital signal execution unit by selecting each general purpose instruction to be transferred to the digital signal execution unit from the shared memory array,
>
> "whereby the selected sequence of individual DSP instructions executed by the digital signal execution unit is selectively configurable by the general purpose processor."

On page 371, in the Introduction section, Crowell discloses that the MC68000 chip is a host processor, while on page 372, column 1, line 9, Crowell teaches that the 74LS241 chips are buffers.

On pages 376-377, Crowell's schematic diagrams show that the address and data lines from the MC68000 processor are connected to the shared bus (the address and data buses A BUS and D BUS) via the buffers (the 74LS241 chips). Thus, when the 74LS241 buffers are turned on, the MC68000 processor is connected to the shared bus (the address and data buses A BUS and D BUS).

In addition, on page 371, in the System Configuration section, Crowell discloses that both instructions and data are transferred from the 68000 host processor to the shared memories (the IMS1421-40 chips), and then to the DSP (the TMS32020 chip). Thus, claim 1 of the '153 patent appears to read on the Crowell document.

With respect to independent claim 9 of the '153 patent, this claim requires:

> "(a) a digital signal execution unit that recovers digital data from the digital signal by

executing a selected sequence of digital signal processor (DSP) instructions;

(b) a general purpose processor that selects the sequence of DSP instructions for execution by the digital signal execution unit from a set of DSP instructions and that performs general purpose processing tasks by executing general purpose instructions utilizing selected data;

(c) a shared internal bus for transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected; and

(d) a shared internal memory array connected to the shared internal bus via an internal input/output port of the shared internal memory array such that the shared internal memory array is accessible by the digital signal execution unit via the internal input/output port for transferring operands utilizable by the digital signal execution unit between the shared internal memory array and the digital signal execution unit on the shared internal bus and such that the shared internal memory array is accessible by the general purpose processor via the internal input/output port for transferring the general purpose instructions and the selected data between the shared internal memory array and the general purpose processor on the shared internal bus;"

The above discussion with respect to the digital signal execution unit, the general purpose processor, the shared internal bus, and the shared internal memory array of claim 1 also apply to claim 9.

Claim 9 of the '153 patent further requires:

"wherein the digital signal execution unit includes an internal address generator for retrieving operands from the shared internal memory array via the shared internal bus for use by the digital signal execution unit in executing the selected sequence of DSP instructions."

On page 12 of the DSPA document, which shows the internal core of the TMS32020 chip, the registers

which are labeled ARO(16), AR1(16), AR2(16), AR3(16), and AR4(16) function as an internal address generator as required by claim 9. Thus, claim 9 of the '153 patent appears to read on page 12 and the Crowell chapter of the DSPA document.

With respect to independent claim 10 of the '153 patent, elements (a), (b), (c), and (d) are the same as the corresponding elements in claim 9. Thus, the above discussion with respect to the digital signal execution unit, the general purpose processor, the shared internal bus, and the shared internal memory array of claim 1 also apply to claim 10.

Claim 10 of the '153 patent further requires:

> "(e) an instruction sequencing unit connected to the shared internal bus for controlling the flow of execution of the DSP instructions and the general purpose instructions."

Although the Crowell document does not explicitly show this unit, it is believed that one skilled in the art would understand that the MC68000 chip has circuitry which performs this function. Thus, claim 10 of the '153 patent further appears to read on the Crowell document.

As a result, claims 1, 9, and 10 are cancelled in this reissue application.

8. I hereby further state that a second error that is being relied upon as a basis for reissue is that none of the claims in the '153 patent provide coverage of the scope provided by new reissue claims 11-44. As a result, I believe the original patent to be wholly or partly inoperative or invalid by reason of my co-inventors and I claiming less than we had a right to claim.

New independent reissue claims 11, 20, and 29 define the invention as follows:

> 11. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register and starting execution of an instruction in response to the GPP loading information into the register.

> 20. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register and executing an instruction in response to the GPP loading information into the register, the information loaded into the register identifying the instruction.

> 29. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register, executing an instruction in response to the GPP loading information into the register, and retrieving operands required by the instruction from the memory by processing the information loaded into the register.

Support for new claims 11, 20, and 29 may be found in FIG. 3, in column 6, lines 37-67, column 8, lines 25-53, and column 9, lines 55-65 of the '153 patent specification.

None of the existing claims provide a scope of coverage which is the same as, or comparable to, the

scope of coverage now provided by new reissue claims 11, 20, and 29. Independent claim 4 and dependent claims 5-6 are the only existing claims that recite a DSP which has a register (a control register). Claims 4-6, however, do not recite that the GPP loads operands into the memory.

In addition, none of the previously submitted claims provided a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 11, 20, and 29. The only previously submitted claims which recite a DSP that has a register are independent claim 10 and dependent claims 11-14 in the originally-filed application (Application Serial No. 07/467,148 filed on January 18, 1990).

Independent claim 10, in addition to reciting a register, also recited an internal memory that provided storage for data retrieved by the GPP. Originally-filed claim 10, however, further recited a number of elements which are not present in new reissue claims 11, 20, and 29; namely a bus interface unit and an external memory. Thus, originally-filed claims 10-14 did not provide a scope of coverage which is the same as, or comparable to, new reissue claims 11, 20, and 29.

Subsequently, originally-filed claim 10 was amended in a Preliminary Amendment filed on January 29, 1993 as part of an FWC application (Application Serial No. 08/011,102 filed on January 29, 1993). The amendment added limitations to originally-filed claim 10, and deleted the bus interface unit, the external memory, and reference to the internal memory providing storage for data retrieved by the GPP.

In addition, dependent claim 11 was also amended to add further limitations to the multiplier/

accumulator unit, while claims 13 and 14 were cancelled (dependent claim 12 further defines the address generator of original claim 10). Thus, claims 10-11, as amended, and claim 12 did not provide a scope of coverage which is the same as, or comparable to, new reissue claims 11, 20, and 29.

Following this, amended claim 10 was cancelled in favor of claim 27 in the Amendment filed on January 7, 1994. In addition, claims 11-12 were amended to further recite the multiply/accumulate unit, and the address generator. Claims 27 and 11-12, in turn, subsequently issued as claims 4-6, respectively, of the '153 patent.

Therefore, none of the existing claims, and none of the previously presented claims, provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 11, 20, and 29.

New dependent reissue claims 12-19, 21-28, and 30-36 further recite the invention as follows:

> 12. The data processing system of claim 11 wherein the operands held in the memory are randomly accessible.
>
> 13. The data processing system of claim 11 wherein the information placed in the register identifies the instruction to be executed.
>
> 14. The data processing system of claim 11 wherein the DSP is connected to the memory via a second bus.
>
> 15. The data processing system of claim 11 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.
>
> 16. The data processing system of claim 11 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

17. The data processing system of claim 11 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

18. The data processing system of claim 11 wherein the DSP only executes a single instruction when said information is loaded into the register.

19. The data processing system of claim 11 wherein the DSP retrieves the operands from the memory.

21. The data processing system of claim 20 wherein the operands held in the memory are randomly accessible.

22. The data processing system of claim 20 wherein the information placed in the register identifies the instruction to be executed.

23. The data processing system of claim 20 wherein the DSP is connected to the memory via a second bus.

24. The data processing system of claim 20 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

25. The data processing system of claim 20 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

26. The data processing system of claim 20 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

27. The data processing system of claim 20 wherein the DSP only executes a single instruction when said information is loaded into the register.

28. The data processing system of claim 20 wherein the DSP retrieves the operands from the memory.

30. The data processing system of claim 29 wherein the operands held in the memory are randomly accessible.

31. The data processing system of claim 29 wherein the information placed in the register identifies the instruction to be executed.

32. The data processing system of claim 29 wherein the DSP is connected to the memory via a second bus.

33. The data processing system of claim 29 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

34. The data processing system of claim 29 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

35. The data processing system of claim 29 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

36. The data processing system of claim 29 wherein the DSP only executes a single instruction when said information is loaded into the register.

Support for new reissue claims 12, 21, and 30 may be found in column 6, lines 5-7 of the '153 patent specification. Support for new reissue claims 13, 22, and 31 may be found in column 6, lines 47-50 and column 9, lines 55-57 of the '153 patent specification. Support for new reissue claims 14, 23, and 32 may be found in FIG. 3 of the '153 patent specification. Support for new reissue claims 15, 24, and 33 may be found in column 6, lines 50-53 of the '153 patent specification. Support for new reissue claims 16-18, 25-27, and 34-36 may be found in column 6, lines 54-67 of the '153 patent specification. Support for new reissue claims 19 and 28 may be found in column 6, lines 45-46.

Since existing claims 4-6 fail to recite that the GPP loads operands into the memory, none of the existing claims provide a scope of coverage which is

the same as, or comparable to, the scope of coverage now provided by new reissue claims 12-19, 21-28, and 30-36.

In addition, since originally-filed claims 10-14 recited elements which are not recited in new reissue claims 12-19, 21-28, and 30-36; and amended claims 10-11 and claim 12 no longer recite that the GPP loads operands into the memory, none of the previously submitted claims provided a scope of coverage which is the same as, or comparable to, new reissue claims 12-19, 21-28, and 30-36.

In addition, new independent reissue claim 37 recites the invention as follows:

> 37. A data processing system comprising:
> a digital signal processor (DSP) that processes digital data by executing an algorithm that includes a specific sequence of DSP operations;
> a general purpose processor (GPP) that selects the sequence of DSP operations for execution by the DSP from a basic set of DSP operations, and that performs general purpose tasks utilizing selected instructions and data;
> a bus to which both the DSP and the GPP are connected;
> a memory connected to the bus such that the memory is accessible by the DSP for retrieving operands utilized by the DSP in executing the selected sequence of DSP operations and by the GPP for loading operands required for execution of the selected DSP algorithm and/or instructions and data for use by the GPP for controlling the DSP; and
> a control register of the DSP characterized in that said GPP invokes a first DSP operation in the selected sequence by issuing a corresponding command directly to said control register of the DSP.

Support for new reissue claim 37 may be found in FIG. 3, and column 6, lines 37-67 of the '153 patent specification.

As with new reissue claims 11, 20, and 29, new reissue claim 37 recites that the GPP loads operands into the memory, and that the DSP has a register, but does not recite either a bus interface unit or an external memory. As a result, none of the existing claims, and none of the previously submitted claims, provide a scope of coverage which is the same as, or comparable to, the scope of coverage provide by new reissue claim 37.

New dependent reissue claims 38-39 further recite the invention as follows:

> 38. The system of claim 37 wherein the DSP, in response to receiving a first DSP operation, places the GPP in a continuous wait state while the DSP performs the first DSP operation utilizing operands retrieved from the memory.
>
> 39. The system of claim 37 wherein, upon completion of execution of the selected sequence of the DSP operations, the GPP downloads contents of the memory and retrieves a new set of operands, instructions, and data for a new sequence of DSP operations.

Support for claims 38-39 may be found in column 8, lines 37-67 of the '153 patent specification.

Since existing claims 4-6 fail to recite that the GPP loads operands into the memory, none of the existing claims provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 38-39.

In addition, since originally-filed claims 10-14 recited elements which are not recited in new reissue claims 38-39, and amended claims 10-11 and claim 12 no longer recite that the GPP loads operands into the memory, none of the previously submitted claims

provided a scope of coverage which is the same as, or comparable to, new reissue claims 38-39.

Further, new independent reissue claim 40 recites the invention as follows:

> 40. A data processing system comprising:
> a first data bus;
> a second data bus;
> a memory connected to the first data bus and the second data bus;
> a general purpose processor (GPP) connected to the first data bus, the GPP loading operands into the memory via the first data bus; and
> a digital signal processor (DSP) connected to the first data bus and the second data bus, the DSP executing an instruction identified by the GPP, and retrieving operands from the memory via the second data bus.

Support for new claim 40 may be found in FIG. 3, and in column 6, lines 37-67 of the '153 patent specification.

None of the existing claims provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claim 40 as none of the existing and previously submitted claims recite a first memory and a DSP that are connected to both a first data bus and a second data bus.

New dependent reissue claims 41-44 further recite the invention as follows:

> 41. The data processing system of claim 40 wherein the operands held in the memory are randomly accessible.

> 42. The data processing system of claim 40 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

> 43. The data processing system of claim 40 wherein the GPP reads a value that results from

executing the instruction after the DSP completes execution of the instruction.

44. The data processing system of claim 40 and further comprising:
a bus interface unit connected to the first data bus; and
a third data bus connected to the bus interface unit.

Support for new reissue claims 41-44 may be found in FIG. 3 and column 6, lines 37-67 of the '153 patent specification.

Since none of the existing claims, and none of the previously presented claims, recite a first memory and a DSP that are connected to both a first data bus and a second data bus, none of the existing claims, and none of the previously presented claims provide the scope of coverage provided by new reissue claims 41-44.

9. All errors being corrected in this reissue application up to the time of filing this declaration arose without any deceptive intention on my part.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such

willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: 16-July-1998 By: _____
Lev Epstein

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of	
Amos Intrater et al.	**DECLARATION OF MAURICE VALENTATEN**
Patent No. 5,630,153	
Issued: May 13, 1997	2001 Ferry Building San Francisco, CA 94111
For: **INTEGRATED DIGITAL SIGNAL PROCESSOR/GENERAL PURPOSE CPU WITH SHARED INTERNAL MEMORY**	(415) 433-4150 Attorney Docket No: NSC8-8400

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

I, Maurice Valentaten, hereby declare that:

1. This declaration is directed to U.S. Patent No. 5,630,153 (the '153 patent), which issued on May 13, 1997.

2. My residence and post office address are both Kurt Huber Ring 3, 82256 Fuerstenfeldbruck, Germany. I am a citizen of Belgium.

3. I am a joint inventor of the invention recited in the claims of the '153 patent. The names, addresses, and citizenships of my co-inventors are:

a. Gideon Intrater. The residence and post office address of Gideon Intrater are both 1035 Aster Ave., Sunnyvale, CA 94086. Gideon Intrater is an Israeli citizen.

b. Amos Intrater. The residence and post office address of Amos Intrater are both 81 Emek Hefer St., Netanya, 42220 Israel. Amos Intrater is an Israeli citizen.

c. Moshe Doron. The residence and post office address of Moshe Doron are both 7 Hashachar St., Raanana, 43564 Israel. Moshe Doron is an Israeli citizen.

d. Lev Epstein. The residence and post office address of Lev Epstein are both 13A Admonit St., Ramat Poleg, Netanya, Israel. Lev Epstein is an Israeli citizen.

e. Israel Greiss. The residence and post office address of Israel Greiss are both 48 Rambam St., Raanana, 43602 Israel. Israel Greiss is an Israeli citizen.

4. I hereby state that I have reviewed and understand the contents of the specification of the '153 patent, including the claims, as amended by any amendments specifically referred to in this declaration.

5. I believe my co-inventors and I are the original and first inventors of the subject matter which is described and claimed in the '153 patent for which a reissue patent is sought.

6. I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37 of the Code of Federal Regulations (CFR) §1.56.

7. I hereby state that one error that is being relied upon as the basis for reissue is that claims 1, 9, and 10 of the '153 patent appear to read on page 12 and Chapter 13, titled TMS32020 and MC68000 Interface, by Charles Crowell, of Digital Signal Processing Applications with the TMS320 Family,

Volume I, Edited by Kun-Shan Lin, Ph.D., dated September 1986, which has not been previously considered by the Patent Office. Page 12 and the Crowell chapter of the Digital Signal Processing Applications (DSPA) document came to our attention after issuance of the '153 patent. A copy of page 12 and the Crowell chapter from the DSPA document are attached in an accompanying IDS.

Page 12 and the Crowell chapter from the DSPA document cited in the IDS are from a June 1989 reprint. I understand that the assignee of the '153 patent, National Semiconductor, has searched for the 1986 document, but has been unable to find it. Although page 12 and the Crowell chapter of the DSPA document cited in the IDS are from a June 1989 reprint, I believe that page 12 and the Crowell chapter of the June 1989 DSPA document are an exact copy of page 12 and the Crowell chapter of the September 1986 DSPA document because the June 1989 reprint was not separately copyrighted, and was printed with 1986 dates throughout the document. I do not believe that documents with a June 1989 publication date are prior art with respect to the '153 patent because my co-inventors and I have an earlier date of conception.

Since claims 1, 9, and 10 appear to read on page 12 and the Crowell chapter of the DSPA document, I believe the original patent to be wholly or partly inoperative or invalid by reason of my co-inventors and I claiming more than we had a right to claim.

Specifically, claim 1 of the '153 patent requires:

> "a shared bus for transferring both data and instructions; [and]

> "a shared memory array for storing both data and general purpose instructions and that is connected for transfer of both data and general purpose instructions between the shared bus and the shared memory array". [Brackets added].

In the schematic diagrams shown on pages 376-377, the Crowell document discloses an address bus A BUS and a data bus D BUS for transferring both data and instructions. In addition, on page 372, column 1, line 11, the Crowell document teaches that the IMS1421-40 chips are shared memories which, as shown on page 377, are connected to the shared bus (the address and data buses A BUS and D BUS). Further, on page 371, in the System Configuration section, Crowell discloses that the shared memories (the IMS1421-40 ships) store both data and instructions.

Claim 1 of the '153 patent also requires:

> "a digital signal execution unit connected to the shared bus for processing the digital signal utilizing both data transferred between the shared memory array and the digital signal execution unit on the shared bus and a selected sequence of individual digital signal processor (DSP) instructions, the selected sequence of DSP instructions consisting of individual general purpose instructions transferred between the shared memory array and the digital signal execution unit on the shared bus".

On page 373, under the Summary section, Crowell teaches that the TMS32020 chip is a digital signal processor (DSP) which, as shown on page 377, is connected to the shared memories (the IMS1421-40 chips) via the shared bus (the address and data buses A BUS and D BUS). Further, on page 371, in the System Configuration section, Crowell discloses that both instructions and data are transferred to the

shared memories (the IMS1421-40 chips) for use by the DSP (the TMS32020 chip).

Claim 1 of the '153 patent further requires:

> "a general purpose processor connected to the shared bus for controlling the digital signal execution unit by selecting each general purpose instruction to be transferred to the digital signal execution unit from the shared memory array,
>
> "whereby the selected sequence of individual DSP instructions executed by the digital signal execution unit is selectively configurable by the general purpose processor."

On page 371, in the Introduction section, Crowell discloses that the MC68000 chip is a host processor, while on page 372, column 1, line 9, Crowell teaches that the 74LS241 chips are buffers.

On pages 376-377, Crowell's schematic diagrams show that the address and data lines from the MC68000 processor are connected to the shared bus (the address and data buses A BUS and D BUS) via the buffers (the 74LS241 chips). Thus, when the 74LS241 buffers are turned on, the MC68000 processor is connected to the shared bus (the address and data buses A BUS and D BUS).

In addition, on page 371, in the System Configuration section, Crowell discloses that both instructions and data are transferred from the 68000 host processor to the shared memories (the IMS1421-40 chips), and then to the DSP (the TMS32020 chip). Thus, claim 1 of the '153 patent appears to read on the Crowell document.

With respect to independent claim 9 of the '153 patent, this claim requires:

> "(a) a digital signal execution unit that recovers digital data from the digital signal by

executing a selected sequence of digital signal processor (DSP) instructions;

(b) a general purpose processor that selects the sequence of DSP instructions for execution by the digital signal execution unit from a set of DSP instructions and that performs general purpose processing tasks by executing general purpose instructions utilizing selected data;

(c) a shared internal bus for transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected; and

(d) a shared internal memory array connected to the shared internal bus via an internal input/output port of the shared internal memory array such that the shared internal memory array is accessible by the digital signal execution unit via the internal input/output port for transferring operands utilizable by the digital signal execution unit between the shared internal memory array and the digital signal execution unit on the shared internal bus and such that the shared internal memory array is accessible by the general purpose processor via the internal input/output port for transferring the general purpose instructions and the selected data between the shared internal memory array and the general purpose processor on the shared internal bus;"

The above discussion with respect to the digital signal execution unit, the general purpose processor, the shared internal bus, and the shared internal memory array of claim 1 also apply to claim 9.

Claim 9 of the '153 patent further requires:

"wherein the digital signal execution unit includes an internal address generator for retrieving operands from the shared internal memory array via the shared internal bus for use by the digital signal execution unit in executing the selected sequence of DSP instructions."

On page 12 of the DSPA document, which shows the internal core of the TMS32020 chip, the registers

which are labeled AR0(16), AR1(16), AR2(16), AR3(16), and AR4(16) function as an internal address generator as required by claim 9. Thus, claim 9 of the '153 patent appears to read on page 12 and the Crowell chapter of the DSPA document.

With respect to independent claim 10 of the '153 patent, elements (a), (b), (c), and (d) are the same as the corresponding elements in claim 9. Thus, the above discussion with respect to the digital signal execution unit, the general purpose processor, the shared internal bus, and the shared internal memory array of claim 1 also apply to claim 10.

Claim 10 of the '153 patent further requires:

> "(e) an instruction sequencing unit connected to the shared internal bus for controlling the flow of execution of the DSP instructions and the general purpose instructions."

Although the Crowell document does not explicitly show this unit, it is believed that one skilled in the art would understand that the MC68000 chip has circuitry which performs this function. Thus, claim 10 of the '153 patent further appears to read on the Crowell document.

As a result, claims 1, 9, and 10 are cancelled in this reissue application.

8. I hereby further state that a second error that is being relied upon as a basis for reissue is that none of the claims in the '153 patent provide coverage of the scope provided by new reissue claims 11-44. As a result, I believe the original patent to be wholly or partly inoperative or invalid by reason of my co-inventors and I claiming less than we had a right to claim.

New independent reissue claims 11, 20, and 29 define the invention as follows:

> 11. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register and starting execution of an instruction in response to the GPP loading information into the register.

> 20. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register and executing an instruction in response to the GPP loading information into the register, the information loaded into the register identifying the instruction.

> 29. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register, executing an instruction in response to the GPP loading information into the register, and retrieving operands required by the instruction from the memory by processing the information loaded into the register.

Support for new claims 11, 20, and 29 may be found in FIG. 3, in column 6, lines 37-67, column 8, lines 25-53, and column 9, lines 55-65 of the '153 patent specification.

None of the existing claims provide a scope of coverage which is the same as, or comparable to, the

scope of coverage now provided by new reissue claims 11, 20, and 29. Independent claim 4 and dependent claims 5-6 are the only existing claims that recite a DSP which has a register (a control register). Claims 4-6, however, do not recite that the GPP loads operands into the memory.

In addition, none of the previously submitted claims provided a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 11, 20, and 29. The only previously submitted claims which recite a DSP that has a register are independent claim 10 and dependent claims 11-14 in the originally-filed application (Application Serial No. 07/467,148 filed on January 18, 1990).

Independent claim 10, in addition to reciting a register, also recited an internal memory that provided storage for data retrieved by the GPP. Originally-filed claim 10, however, further recited a number of elements which are not present in new reissue claims 11, 20, and 29; namely a bus interface unit and an external memory. Thus, originally-filed claims 10-14 did not provide a scope of coverage which is the same as, or comparable to, new reissue claims 11, 20, and 29.

Subsequently, originally-filed claim 10 was amended in a Preliminary Amendment filed on January 29, 1993 as part of an FWC application (Application Serial No. 08/011,102 filed on January 29, 1993). The amendment added limitations to originally-filed claim 10, and deleted the bus interface unit, the external memory, and reference to the internal memory providing storage for data retrieved by the GPP.

In addition, dependent claim 11 was also amended to add further limitations to the multiplier/

accumulator unit, while claims 13 and 14 were cancelled (dependent claim 12 further defines the address generator of original claim 10). Thus, claims 10-11, as amended, and claim 12 did not provide a scope of coverage which is the same as, or comparable to, new reissue claims 11, 20, and 29.

Following this, amended claim 10 was cancelled in favor of claim 27 in the Amendment filed on January 7, 1994. In addition, claims 11-12 were amended to further recite the multiply/accumulate unit, and the address generator. Claims 27 and 11-12, in turn, subsequently issued as claims 4-6, respectively, of the '153 patent.

Therefore, none of the existing claims, and none of the previously presented claims, provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 11, 20, and 29.

New dependent reissue claims 12-19, 21-28, and 30-36 further recite the invention as follows:

> 12. The data processing system of claim 11 wherein the operands held in the memory are randomly accessible.
>
> 13. The data processing system of claim 11 wherein the information placed in the register identifies the instruction to be executed.
>
> 14. The data processing system of claim 11 wherein the DSP is connected to the memory via a second bus.
>
> 15. The data processing system of claim 11 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.
>
> 16. The data processing system of claim 11 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

17. The data processing system of claim 11 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

18. The data processing system of claim 11 wherein the DSP only executes a single instruction when said information is loaded into the register.

19. The data processing system of claim 11 wherein the DSP retrieves the operands from the memory.

21. The data processing system of claim 20 wherein the operands held in the memory are randomly accessible.

22. The data processing system of claim 20 wherein the information placed in the register identifies the instruction to be executed.

23. The data processing system of claim 20 wherein the DSP is connected to the memory via a second bus.

24. The data processing system of claim 20 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

25. The data processing system of claim 20 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

26. The data processing system of claim 20 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

27. The data processing system of claim 20 wherein the DSP only executes a single instruction when said information is loaded into the register.

28. The data processing system of claim 20 wherein the DSP retrieves the operands from the memory.

30. The data processing system of claim 29 wherein the operands held in the memory are randomly accessible.

31. The data processing system of claim 29 wherein the information placed in the register identifies the instruction to be executed.

32. The data processing system of claim 29 wherein the DSP is connected to the memory via a second bus.

33. The data processing system of claim 29 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

34. The data processing system of claim 29 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

35. The data processing system of claim 29 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

36. The data processing system of claim 29 wherein the DSP only executes a single instruction when said information is loaded into the register.

Support for new reissue claims 12, 21, and 30 may be found in column 6, lines 5-7 of the '153 patent specification. Support for new reissue claims 13, 22, and 31 may be found in column 6, lines 47-50 and column 9, lines 55-57 of the '153 patent specification. Support for new reissue claims 14, 23, and 32 may be found in FIG. 3 of the '153 patent specification. Support for new reissue claims 15, 24, and 33 may be found in column 6, lines 50-53 of the '153 patent specification. Support for new reissue claims 16-18, 25-27, and 34-36 may be found in column 6, lines 54-67 of the '153 patent specification. Support for new reissue claims 19 and 28 may be found in column 6, lines 45-46.

Since existing claims 4-6 fail to recite that the GPP loads operands into the memory, none of the existing claims provide a scope of coverage which is

the same as, or comparable to, the scope of coverage now provided by new reissue claims 12-19, 21-28, and 30-36.

In addition, since originally-filed claims 10-14 recited elements which are not recited in new reissue claims 12-19, 21-28, and 30-36; and amended claims 10-11 and claim 12 no longer recite that the GPP loads operands into the memory, none of the previously submitted claims provided a scope of coverage which is the same as, or comparable to, new reissue claims 12-19, 21-28, and 30-36.

In addition, new independent reissue claim 37 recites the invention as follows:

> 37. A data processing system comprising:
> a digital signal processor (DSP) that processes digital data by executing an algorithm that includes a specific sequence of DSP operations;
> a general purpose processor (GPP) that selects the sequence of DSP operations for execution by the DSP from a basic set of DSP operations, and that performs general purpose tasks utilizing selected instructions and data;
> a bus to which both the DSP and the GPP are connected;
> a memory connected to the bus such that the memory is accessible by the DSP for retrieving operands utilized by the DSP in executing the selected sequence of DSP operations and by the GPP for loading operands required for execution of the selected DSP algorithm and/or instructions and data for use by the GPP for controlling the DSP; and
> a control register of the DSP characterized in that said GPP invokes a first DSP operation in the selected sequence by issuing a corresponding command directly to said control register of the DSP.

Support for new reissue claim 37 may be found in FIG. 3, and column 6, lines 37-67 of the '153 patent specification.

As with new reissue claims 11, 20, and 29, new reissue claim 37 recites that the GPP loads operands into the memory, and that the DSP has a register, but does not recite either a bus interface unit or an external memory. As a result, none of the existing claims, and none of the previously submitted claims, provide a scope of coverage which is the same as, or comparable to, the scope of coverage provide by new reissue claim 37.

New dependent reissue claims 38-39 further recite the invention as follows:

> 38. The system of claim 37 wherein the DSP, in response to receiving a first DSP operation, places the GPP in a continuous wait state while the DSP performs the first DSP operation utilizing operands retrieved from the memory.
>
> 39. The system of claim 37 wherein, upon completion of execution of the selected sequence of the DSP operations, the GPP downloads contents of the memory and retrieves a new set of operands, instructions, and data for a new sequence of DSP operations.

Support for claims 38-39 may be found in column 8, lines 37-67 of the '153 patent specification.

Since existing claims 4-6 fail to recite that the GPP loads operands into the memory, none of the existing claims provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 38-39.

In addition, since originally-filed claims 10-14 recited elements which are not recited in new reissue claims 38-39, and amended claims 10-11 and claim 12 no longer recite that the GPP loads operands into the memory, none of the previously submitted claims

provided a scope of coverage which is the same as, or comparable to, new reissue claims 38-39.

Further, new independent reissue claim 40 recites the invention as follows:

> 40. A data processing system comprising:
> a first data bus;
> a second data bus;
> a memory connected to the first data bus and the second data bus;
> a general purpose processor (GPP) connected to the first data bus, the GPP loading operands into the memory via the first data bus; and
> a digital signal processor (DSP) connected to the first data bus and the second data bus, the DSP executing an instruction identified by the GPP, and retrieving operands from the memory via the second data bus.

Support for new claim 40 may be found in FIG. 3, and in column 6, lines 37-67 of the '153 patent specification.

None of the existing claims provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claim 40 as none of the existing and previously submitted claims recite a first memory and a DSP that are connected to both a first data bus and a second data bus.

New dependent reissue claims 41-44 further recite the invention as follows:

> 41. The data processing system of claim 40 wherein the operands held in the memory are randomly accessible.
>
> 42. The data processing system of claim 40 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.
>
> 43. The data processing system of claim 40 wherein the GPP reads a value that results from

executing the instruction after the DSP completes execution of the instruction.

44. The data processing system of claim 40 and further comprising:
a bus interface unit connected to the first data bus; and
a third data bus connected to the bus interface unit.

Support for new reissue claims 41-44 may be found in FIG. 3 and column 6, lines 37-67 of the '153 patent specification.

Since none of the existing claims, and none of the previously presented claims, recite a first memory and a DSP that are connected to both a first data bus and a second data bus, none of the existing claims, and none of the previously presented claims provide the scope of coverage provided by new reissue claims 41-44.

9. All errors being corrected in this reissue application up to the time of filing this declaration arose without any deceptive intention on my part.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such

willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: 27/08/98
08/27/98

By: ______________________
Maurice Valentaten

Express Mail Label No.:
EL151571733US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of	
Amos Intrater et al.	**DECLARATION OF ISRAEL GREISS**
Patent No. 5,630,153	
Issued: May 13, 1997	2001 Ferry Building San Francisco, CA 94111 (415) 433-4150
For: **INTEGRATED DIGITAL SIGNAL PROCESSOR/GENERAL PURPOSE CPU WITH SHARED INTERNAL MEMORY**	Attorney Docket No: NSC8-8400

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

I, Israel Greiss, hereby declare that:

1. This declaration is directed to U.S. Patent No. 5,630,153 (the '153 patent), which issued on May 13, 1997.

2. My residence and post office address are both 48 Rambam St., Raanana, 43602 Israel. I am a citizen of Israel.

3. I am a joint inventor of the invention recited in the claims of the '153 patent. The names, addresses, and citizenships of my co-inventors are:

a. Gideon Intrater. The residence and post office address of Gideon Intrater are both 1035 Aster Ave., Sunnyvale, CA 94086. Gideon Intrater is an Israeli citizen.

b. Amos Intrater. The residence and post office address of Amos Intrater are both 81 Emek Hefer St., Netanya, 42220 Israel. Amos Intrater is an Israeli citizen.

c. Moshe Doron. The residence and post office address of Moshe Doron are both 7 Hashachar St., Raanana, 43564 Israel. Moshe Doron is an Israeli citizen.

d. Lev Epstein. The residence and post office address of Lev Epstein are both 13A Admonit St., Ramat Poleg, Netanya, Israel. Lev Epstein is an Israeli citizen.

e. Maurice Valentaten. The residence and post office address of Maurice Valentaten are both Kurt Huber Ring 3, 82256 Fuerstenfeldbruck, Germany. Maurice Valentaten is a Belgian citizen.

4. I hereby state that I have reviewed and understand the contents of the specification of the '153 patent, including the claims, as amended by any amendments specifically referred to in this declaration.

5. I believe my co-inventors and I are the original and first inventors of the subject matter which is described and claimed in the '153 patent for which a reissue patent is sought.

6. I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37 of the Code of Federal Regulations (CFR) §1.56.

7. I hereby state that one error that is being relied upon as the basis for reissue is that claims 1, 9, and 10 of the '153 patent appear to read on page 12 and Chapter 13, titled TMS32020 and MC68000 Interface, by Charles Crowell, of Digital Signal

Processing Applications with the TMS320 Family, Volume I, Edited by Kun-Shan Lin, Ph.D., dated September 1986, which has not been previously considered by the Patent Office. Page 12 and the Crowell chapter of the Digital Signal Processing Applications (DSPA) document came to our attention after issuance of the '153 patent. A copy of page 12 and the Crowell chapter from the DSPA document are attached in an accompanying IDS.

Page 12 and the Crowell chapter from the DSPA document cited in the IDS are from a June 1989 reprint. I understand that the assignee of the '153 patent, National Semiconductor, has searched for the 1986 document, but has been unable to find it. Although page 12 and the Crowell chapter of the DSPA document cited in the IDS are from a June 1989 reprint, I believe that page 12 and the Crowell chapter of the June 1989 DSPA document are an exact copy of page 12 and the Crowell chapter of the September 1986 DSPA document because the June 1989 reprint was not separately copyrighted, and was printed with 1986 dates throughout the document. I do not believe that documents with a June 1989 publication date are prior art with respect to the '153 patent because my co-inventors and I have an earlier date of conception.

Since claims 1, 9, and 10 appear to read on page 12 and the Crowell chapter of the DSPA document, I believe the original patent to be wholly or partly inoperative or invalid by reason of my co-inventors and I claiming more than we had a right to claim.

Specifically, claim 1 of the '153 patent requires:

> "a shared bus for transferring both data and instructions; [and]

> "a shared memory array for storing both data and general purpose instructions and that is connected for transfer of both data and general purpose instructions between the shared bus and the shared memory array". [Brackets added].

In the schematic diagrams shown on pages 376-377, the Crowell document discloses an address bus A BUS and a data bus D BUS for transferring both data and instructions. In addition, on page 372, column 1, line 11, the Crowell document teaches that the IMS1421-40 chips are shared memories which, as shown on page 377, are connected to the shared bus (the address and data buses A BUS and D BUS). Further, on page 371, in the System Configuration section, Crowell discloses that the shared memories (the IMS1421-40 ships) store both data and instructions.

Claim 1 of the '153 patent also requires:

> "a digital signal execution unit connected to the shared bus for processing the digital signal utilizing both data transferred between the shared memory array and the digital signal execution unit on the shared bus and a selected sequence of individual digital signal processor (DSP) instructions, the selected sequence of DSP instructions consisting of individual general purpose instructions transferred between the shared memory array and the digital signal execution unit on the shared bus".

On page 373, under the Summary section, Crowell teaches that the TMS32020 chip is a digital signal processor (DSP) which, as shown on page 377, is connected to the shared memories (the IMS1421-40 chips) via the shared bus (the address and data buses A BUS and D BUS). Further, on page 371, in the System Configuration section, Crowell discloses that both instructions and data are transferred to the

shared memories (the IMS1421-40 chips) for use by the DSP (the TMS32020 chip).

Claim 1 of the '153 patent further requires:

> "a general purpose processor connected to the shared bus for controlling the digital signal execution unit by selecting each general purpose instruction to be transferred to the digital signal execution unit from the shared memory array,
>
> "whereby the selected sequence of individual DSP instructions executed by the digital signal execution unit is selectively configurable by the general purpose processor."

On page 371, in the Introduction section, Crowell discloses that the MC68000 chip is a host processor, while on page 372, column 1, line 9, Crowell teaches that the 74LS241 chips are buffers.

On pages 376-377, Crowell's schematic diagrams show that the address and data lines from the MC68000 processor are connected to the shared bus (the address and data buses A BUS and D BUS) via the buffers (the 74LS241 chips). Thus, when the 74LS241 buffers are turned on, the MC68000 processor is connected to the shared bus (the address and data buses A BUS and D BUS).

In addition, on page 371, in the System Configuration section, Crowell discloses that both instructions and data are transferred from the 68000 host processor to the shared memories (the IMS1421-40 chips), and then to the DSP (the TMS32020 chip). Thus, claim 1 of the '153 patent appears to read on the Crowell document.

With respect to independent claim 9 of the '153 patent, this claim requires:

> "(a) a digital signal execution unit that recovers digital data from the digital signal by

executing a selected sequence of digital signal processor (DSP) instructions;

(b) a general purpose processor that selects the sequence of DSP instructions for execution by the digital signal execution unit from a set of DSP instructions and that performs general purpose processing tasks by executing general purpose instructions utilizing selected data;

(c) a shared internal bus for transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected; and

(d) a shared internal memory array connected to the shared internal bus via an internal input/output port of the shared internal memory array such that the shared internal memory array is accessible by the digital signal execution unit via the internal input/output port for transferring operands utilizable by the digital signal execution unit between the shared internal memory array and the digital signal execution unit on the shared internal bus and such that the shared internal memory array is accessible by the general purpose processor via the internal input/output port for transferring the general purpose instructions and the selected data between the shared internal memory array and the general purpose processor on the shared internal bus;"

The above discussion with respect to the digital signal execution unit, the general purpose processor, the shared internal bus, and the shared internal memory array of claim 1 also apply to claim 9.

Claim 9 of the '153 patent further requires:

"wherein the digital signal execution unit includes an internal address generator for retrieving operands from the shared internal memory array via the shared internal bus for use by the digital signal execution unit in executing the selected sequence of DSP instructions."

On page 12 of the DSPA document, which shows the internal core of the TMS32020 chip, the registers

which are labeled AR0(16), AR1(16), AR2(16), AR3(16), and AR4(16) function as an internal address generator as required by claim 9. Thus, claim 9 of the '153 patent appears to read on page 12 and the Crowell chapter of the DSPA document.

With respect to independent claim 10 of the '153 patent, elements (a), (b), (c), and (d) are the same as the corresponding elements in claim 9. Thus, the above discussion with respect to the digital signal execution unit, the general purpose processor, the shared internal bus, and the shared internal memory array of claim 1 also apply to claim 10.

Claim 10 of the '153 patent further requires:

> "(e) an instruction sequencing unit connected to the shared internal bus for controlling the flow of execution of the DSP instructions and the general purpose instructions."

Although the Crowell document does not explicitly show this unit, it is believed that one skilled in the art would understand that the MC68000 chip has circuitry which performs this function. Thus, claim 10 of the '153 patent further appears to read on the Crowell document.

As a result, claims 1, 9, and 10 are cancelled in this reissue application.

8. I hereby further state that a second error that is being relied upon as a basis for reissue is that none of the claims in the '153 patent provide coverage of the scope provided by new reissue claims 11-44. As a result, I believe the original patent to be wholly or partly inoperative or invalid by reason of my co-inventors and I claiming less than we had a right to claim.

New independent reissue claims 11, 20, and 29 define the invention as follows:

> 11. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register and starting execution of an instruction in response to the GPP loading information into the register.

> 20. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register and executing an instruction in response to the GPP loading information into the register, the information loaded into the register identifying the instruction.

> 29. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register, executing an instruction in response to the GPP loading information into the register, and retrieving operands required by the instruction from the memory by processing the information loaded into the register.

Support for new claims 11, 20, and 29 may be found in FIG. 3, in column 6, lines 37-67, column 8, lines 25-53, and column 9, lines 55-65 of the '153 patent specification.

None of the existing claims provide a scope of coverage which is the same as, or comparable to, the

scope of coverage now provided by new reissue claims 11, 20, and 29. Independent claim 4 and dependent claims 5-6 are the only existing claims that recite a DSP which has a register (a control register). Claims 4-6, however, do not recite that the GPP loads operands into the memory.

In addition, none of the previously submitted claims provided a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 11, 20, and 29. The only previously submitted claims which recite a DSP that has a register are independent claim 10 and dependent claims 11-14 in the originally-filed application (Application Serial No. 07/467,148 filed on January 18, 1990).

Independent claim 10, in addition to reciting a register, also recited an internal memory that provided storage for data retrieved by the GPP. Originally-filed claim 10, however, further recited a number of elements which are not present in new reissue claims 11, 20, and 29; namely a bus interface unit and an external memory. Thus, originally-filed claims 10-14 did not provide a scope of coverage which is the same as, or comparable to, new reissue claims 11, 20, and 29.

Subsequently, originally-filed claim 10 was amended in a Preliminary Amendment filed on January 29, 1993 as part of an FWC application (Application Serial No. 08/011,102 filed on January 29, 1993). The amendment added limitations to originally-filed claim 10, and deleted the bus interface unit, the external memory, and reference to the internal memory providing storage for data retrieved by the GPP.

In addition, dependent claim 11 was also amended to add further limitations to the multiplier/

accumulator unit, while claims 13 and 14 were cancelled (dependent claim 12 further defines the address generator of original claim 10). Thus, claims 10-11, as amended, and claim 12 did not provide a scope of coverage which is the same as, or comparable to, new reissue claims 11, 20, and 29.

Following this, amended claim 10 was cancelled in favor of claim 27 in the Amendment filed on January 7, 1994. In addition, claims 11-12 were amended to further recite the multiply/accumulate unit, and the address generator. Claims 27 and 11-12, in turn, subsequently issued as claims 4-6, respectively, of the '153 patent.

Therefore, none of the existing claims, and none of the previously presented claims, provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 11, 20, and 29.

New dependent reissue claims 12-19, 21-28, and 30-36 further recite the invention as follows:

> 12. The data processing system of claim 11 wherein the operands held in the memory are randomly accessible.
>
> 13. The data processing system of claim 11 wherein the information placed in the register identifies the instruction to be executed.
>
> 14. The data processing system of claim 11 wherein the DSP is connected to the memory via a second bus.
>
> 15. The data processing system of claim 11 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.
>
> 16. The data processing system of claim 11 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

17. The data processing system of claim 11 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

18. The data processing system of claim 11 wherein the DSP only executes a single instruction when said information is loaded into the register.

19. The data processing system of claim 11 wherein the DSP retrieves the operands from the memory.

21. The data processing system of claim 20 wherein the operands held in the memory are randomly accessible.

22. The data processing system of claim 20 wherein the information placed in the register identifies the instruction to be executed.

23. The data processing system of claim 20 wherein the DSP is connected to the memory via a second bus.

24. The data processing system of claim 20 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

25. The data processing system of claim 20 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

26. The data processing system of claim 20 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

27. The data processing system of claim 20 wherein the DSP only executes a single instruction when said information is loaded into the register.

28. The data processing system of claim 20 wherein the DSP retrieves the operands from the memory.

30. The data processing system of claim 29 wherein the operands held in the memory are randomly accessible.

31. The data processing system of claim 29 wherein the information placed in the register identifies the instruction to be executed.

32. The data processing system of claim 29 wherein the DSP is connected to the memory via a second bus.

33. The data processing system of claim 29 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

34. The data processing system of claim 29 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

35. The data processing system of claim 29 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

36. The data processing system of claim 29 wherein the DSP only executes a single instruction when said information is loaded into the register.

Support for new reissue claims 12, 21, and 30 may be found in column 6, lines 5-7 of the '153 patent specification. Support for new reissue claims 13, 22, and 31 may be found in column 6, lines 47-50 and column 9, lines 55-57 of the '153 patent specification. Support for new reissue claims 14, 23, and 32 may be found in FIG. 3 of the '153 patent specification. Support for new reissue claims 15, 24, and 33 may be found in column 6, lines 50-53 of the '153 patent specification. Support for new reissue claims 16-18, 25-27, and 34-36 may be found in column 6, lines 54-67 of the '153 patent specification. Support for new reissue claims 19 and 28 may be found in column 6, lines 45-46.

Since existing claims 4-6 fail to recite that the GPP loads operands into the memory, none of the existing claims provide a scope of coverage which is

the same as, or comparable to, the scope of coverage now provided by new reissue claims 12-19, 21-28, and 30-36.

In addition, since originally-filed claims 10-14 recited elements which are not recited in new reissue claims 12-19, 21-28, and 30-36; and amended claims 10-11 and claim 12 no longer recite that the GPP loads operands into the memory, none of the previously submitted claims provided a scope of coverage which is the same as, or comparable to, new reissue claims 12-19, 21-28, and 30-36.

In addition, new independent reissue claim 37 recites the invention as follows:

> 37. A data processing system comprising:
> a digital signal processor (DSP) that processes digital data by executing an algorithm that includes a specific sequence of DSP operations;
> a general purpose processor (GPP) that selects the sequence of DSP operations for execution by the DSP from a basic set of DSP operations, and that performs general purpose tasks utilizing selected instructions and data;
> a bus to which both the DSP and the GPP are connected;
> a memory connected to the bus such that the memory is accessible by the DSP for retrieving operands utilized by the DSP in executing the selected sequence of DSP operations and by the GPP for loading operands required for execution of the selected DSP algorithm and/or instructions and data for use by the GPP for controlling the DSP; and
> a control register of the DSP characterized in that said GPP invokes a first DSP operation in the selected sequence by issuing a corresponding command directly to said control register of the DSP.

Support for new reissue claim 37 may be found in FIG. 3, and column 6, lines 37-67 of the '153 patent specification.

As with new reissue claims 11, 20, and 29, new reissue claim 37 recites that the GPP loads operands into the memory, and that the DSP has a register, but does not recite either a bus interface unit or an external memory. As a result, none of the existing claims, and none of the previously submitted claims, provide a scope of coverage which is the same as, or comparable to, the scope of coverage provide by new reissue claim 37.

New dependent reissue claims 38-39 further recite the invention as follows:

> 38. The system of claim 37 wherein the DSP, in response to receiving a first DSP operation, places the GPP in a continuous wait state while the DSP performs the first DSP operation utilizing operands retrieved from the memory.
>
> 39. The system of claim 37 wherein, upon completion of execution of the selected sequence of the DSP operations, the GPP downloads contents of the memory and retrieves a new set of operands, instructions, and data for a new sequence of DSP operations.

Support for claims 38-39 may be found in column 8, lines 37-67 of the '153 patent specification.

Since existing claims 4-6 fail to recite that the GPP loads operands into the memory, none of the existing claims provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 38-39.

In addition, since originally-filed claims 10-14 recited elements which are not recited in new reissue claims 38-39, and amended claims 10-11 and claim 12 no longer recite that the GPP loads operands into the memory, none of the previously submitted claims

provided a scope of coverage which is the same as, or comparable to, new reissue claims 38-39.

Further, new independent reissue claim 40 recites the invention as follows:

> 40. A data processing system comprising:
> a first data bus;
> a second data bus;
> a memory connected to the first data bus and the second data bus;
> a general purpose processor (GPP) connected to the first data bus, the GPP loading operands into the memory via the first data bus; and
> a digital signal processor (DSP) connected to the first data bus and the second data bus, the DSP executing an instruction identified by the GPP, and retrieving operands from the memory via the second data bus.

Support for new claim 40 may be found in FIG. 3, and in column 6, lines 37-67 of the '153 patent specification.

None of the existing claims provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claim 40 as none of the existing and previously submitted claims recite a first memory and a DSP that are connected to both a first data bus and a second data bus.

New dependent reissue claims 41-44 further recite the invention as follows:

> 41. The data processing system of claim 40 wherein the operands held in the memory are randomly accessible.
>
> 42. The data processing system of claim 40 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.
>
> 43. The data processing system of claim 40 wherein the GPP reads a value that results from

executing the instruction after the DSP completes execution of the instruction.

44. The data processing system of claim 40 and further comprising:
a bus interface unit connected to the first data bus; and
a third data bus connected to the bus interface unit.

Support for new reissue claims 41-44 may be found in FIG. 3 and column 6, lines 37-67 of the '153 patent specification.

Since none of the existing claims, and none of the previously presented claims, recite a first memory and a DSP that are connected to both a first data bus and a second data bus, none of the existing claims, and none of the previously presented claims provide the scope of coverage provided by new reissue claims 41-44.

9. All errors being corrected in this reissue application up to the time of filing this declaration arose without any deceptive intention on my part.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such

willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: 11/25/93 By: ____________________
Israel Greiss